DRAFT- 2-16-2025

IEEE SOLID-STATE CIRCUITS SOCIETY

ADVANCE PROGRAM

2025 IEEE INTERNATIONAL SOLID-STATE CIRCUITS CONFERENCE

FEBRUARY 16, 17, 18, 19, 20

CONFERENCE THEME:

The Silicon Engine Driving the AI Revolution

SAN FRANCISCO
MARRIOTT MARQUIS HOTEL

5-DAY PROGRAM

SUNDAY ALL-DAY

2 FORUMS: Techniques/New Approaches for Die-to-Die Links; Wireless Comm Tech for Space Applications

10 TUTORIALS: Low-noise current sensing; DRAM I/O; Cryo-CMOS for Quantum Computing; Nanopower/Energy Harvesting; RF System Analysis; High-Speed Optical Transceivers; High-Speed A-Digital Converters; Intelligent Neural Interfaces; Generative AI on Edge; mm-Wave Oscillator Design

2 EVENING EVENTS: Bingo Networking; Student Research Preview

THURSDAY ALL-DAY

4 FORUMS: Building Blocks/Compute/Movement/Integration; Data Converter R&D; Advances in Image/Vision Sensing; Evolution of the Software Defined Vehicle

SHORT-COURSE: Wireless/RF Transceiver Circuits

ISSCC VISION STATEMENT

The International Solid-State Circuits Conference is the foremost global forum for presentation of advances in solid-state circuits and systems-on-a-chip. The Conference offers a unique opportunity for engineers working at the cutting edge of IC design and application to maintain technical currency, and to network with leading experts.

CONFERENCE TECHNICAL HIGHLIGHTS

On Sunday, February 16th, the day before the official opening of the Conference, ISSCC 2025 offers:

- A choice of 10 Tutorials, or
- A choice of 1 of 2 all-day Advanced-Circuit-Design Forums:
  "Unlocking Innovation: Circuit Techniques and New Approaches for Die-to-Die Links and the Chiplet Ecosystem"
  "Wireless Communication Technology for Space Applications: From Satellite to Dish and Smartphones"

The 90-minute tutorials offer background information and a review of the basics in specific circuit- and system-design topics. In the all-day Advanced-Circuit-Design Forums, leading experts present state-of-the-art design strategies in a workshop-like format. The Forums are targeted at designers experienced in the technical field.

On Sunday, February 16th, there are two events: "Mentoring Session/Networking Bingo" will be offered starting at 4:00 pm. In addition, the Student-Research Preview (SRP), featuring sixty-second introductory presentations followed by a poster session from selected graduate-student researchers from around the world will begin at 8:00 pm. The SRP will start with an inspirational lecture by Professor Jan Rabaey (UC Berkeley).

On Monday, February 17th, ISSCC 2025 at 8:00 am offers four plenary papers on the theme: ***"The Silicon Engine Driving Driving the AI Revolution"***

On Monday at 1:30 pm, there are five parallel technical sessions, followed by a Social Hour at 5:30 pm open to all ISSCC attendees. The Social Hour, held in conjunction with Book Displays and Author Interviews, will also include a Demonstration Session, featuring posters and live demonstrations of selected papers.

On Tuesday, February 18th, there are six parallel technical sessions, both morning and afternoon. Book Displays and Author Interviews will be accompanied by a second Demonstration Session. Tuesday evening includes three events, entitled:

"Quantum Computing: Whose Qubit is Better?"
"Future of Analog Design: Still Magical or Mostly Digital"
"The Next Decade of AI – Barriers, Opportunities, & Directions"

On Wednesday, February 19th , there will be five parallel technical sessions, both morning and afternoon, followed by Author Interviews.

On Thursday, February 20th, ISSCC offers a choice of five all-day events:

- A Short Course entitled:
  "Advances in Wireless and RF Transceiver Circuits"

- Four Advanced-Circuit-Design Forums entitled:
  "It's all About Data: Building Blocks, Compute, Movement and Integration"
  "Highlights of Data Converter R&D in the Past 5 Years: A Comprehensive Overview"
  "Seeing the Future: Advances in Image and Vision Sensing"
  "Evolution of the Software Defined Vehicle: Navigating Smart Cockpits and In-Car Hardware"

This year, again, there is an option that allows an attendee to sample parts of all 5 Thursday offerings. Registration for educational events on Sunday and Thursday will be filled on a first-come first-served basis. Use of the ISSCC Web-Registration Site (http://www.isscc.org) is strongly encouraged. Registrants will be provided with immediate confirmation on registration for the Conference, Tutorials, Forums, and the Short Course.

Need Additional Information? Go to: www.isscc.org

TABLE OF CONTENTS

ISSCC 2025 SCHEDULE OF EVENTS

Optional Educational Events

ISSCC 2025 • Sunday, February 16th

Tutorials

8:30 AM

T1: Low-Noise Current Sensing

T2: Fundamentals of DRAM I/O: Standards and Circuits

T3: Fundamentals of Cryo-CMOS Circuits and Systems for Quantum Computing

10:30 AM

T4: Fundamental Circuits for Nanopower and Energy-Harvesting Applications

T5: Fundamentals of RF System Analysis for IC Designers

T6: Front-End Circuit Design for High-Speed Optical Transceivers

1:30 PM

T7: High-Speed Analog-to-Digital Converters

T8: Intelligent Neural Interfaces: Fundamentals and Future Directions

3:30 PM

T9: Generative AI on Edge Devices: Models, Hardware and Systems

T10: mm-Wave Oscillator Design

ISSCC 2025 • Sunday, February 16th

Forums

8:00 AM

F1: Unlocking Innovation: Circuit Techniques and New Approaches for Die-to-Die Links and the Chiplet Ecosystem

F2: Wireless Communication Technology for Space Applications: From Satellite to Dish and Smartphones

Events Below are Included with your Conference Registration

ISSCC 2025 • Sunday, February 16th

Evening Events

4:00 PM to 6:00 PM:
Bingo Networking Event (Open to All)

8:00 PM

EE1: Student Research Preview: Short Presentations with Poster Session

ISSCC 2025 SCHEDULE OF EVENTS

Events Below are Included with your Conference Registration

ISSCC 2025 • Monday, February 17th Paper Sessions

8:30 AM	**Session 1:** Plenary - Invited Papers
1:30 PM	**Session 2:** Processors
1:30 PM	**Session 3:** Amplifiers and Analog Front-Ends
3:35 PM	**Session 4:** Analog Techniques
1:30 PM	**Session 5:** Front-End Circuits for High-Performance Transceivers
1:30 PM	**Session 6:** Imagers and Displays
1:30 PM	**Session 7:** Ultra-High-Speed Wireline

3:00 PM to 8:00 PM – Book Displays
3:00 PM to 8:00 PM – Corporations/Institution Exhibition
5:00 PM to 7:00 PM – Demonstration Session
5:30 PM – Author Interviews • Social Hour

ISSCC 2025 • Tuesday, February 18th Paper Sessions

8:00 AM	**Session 8:** Digital Techniques for System Adaptation, Power Management and Clocking
8:00 AM	**Session 9:** Ubiquitous Power Delivery
8:00 AM	**Session 10:** Transceiver Chipsets for Communications and Radar
10:05 AM	**Session 11:** RF and mm-Wave Wireless Receivers
8:00 AM	**Session 12:** Innovations from Outside the (ISSCC's) Box
10:05 AM	**Session 13:** Cool Computation Circuits
8:00 AM	**Session 14:** Compute-in-Memory
8:00 AM	**Session 15:** Neural Interfaces and Edge Intelligence for Medical Devices
1:30 PM	**Session 16:** Invited Industry
3:35 PM	**Session 17:** Hardware Security
1:30 PM	**Session 18:** Noise-Shaping and SAR-Based ADCs
1:30 PM	**Session 19:** Frequency Synthesizers and Series-Resonance VCOs
1:30 PM	**Session 20:** Sensors and Actuators for Health & Autonomy
1:30 PM	**Session 21:** Compute and USB Power
3:35 PM	**Session 22:** Memory Interface

9:30 AM to 1:30 PM – Book Displays
9:30 AM to 1:30 PM – Corporations/Institution Exhibition
3:00 PM to 8:00 PM – Book Displays
3:00 PM to 8:00 PM – Corporations/Institution Exhibition
5:00 PM to 7:00 PM – Demonstration Session
5:30 PM – Author Interviews • Social Hour

ISSCC 2025 • Tuesday, February 18th

Evening Events

8:00 PM

EE2: Quantum Computing: Whose Qubit is Better?
EE3: Future of Analog Design: Still Magical or Mostly Digital?
EE4: The Next Decade of AI – Barriers, Opportunities, & Directions

ISSCC 2025 SCHEDULE OF EVENTS

Events Below are Included with your Conference Registration

ISSCC 2025 • Wednesday, February 19th Paper Sessions

8:00 AM	**Session 23:** AI-Accelerators
8:00 AM	**Session 24:** High-Frequency ADCs
8:00 AM	**Session 25:** High-Concepts at High Frequencies
10:05 AM	**Session 26:** Wireless Transmitters and Front-Ends
8:00 AM	**Session 27:** Sensor Interfaces
10:05 AM	**Session 28:** Capacitive Sensor Readout
8:00 AM	**Session 29:** SRAM
10:05 AM	**Session 30:** Nonvolatile Memory and DRAM
1:30 PM	**Session 31:** Energy Harvesting and IoT Power
3:35 PM	**Session 32:** Isolated Power and Gate Drivers
1:30 PM	**Session 33:** Components for Beyond 100GHz
3:35 PM	**Session 34:** Digital PLLs and Waveform-Shaping VCOs
1:30 PM	**Session 35:** Implantable and Wearable Biomedical Devices
1:30 PM	**Session 36:** Ultra-High-Density D2D and High-Performance Optical Transceivers
1:30 PM	**Session 37:** Design-Technology Optimization and Digital Accelerators

10:00 AM to 3:00 PM – Book Displays
5:30 PM – Author Interviews

Optional Educational Events

ISSCC 2025 • Thursday, February 20th

Forums

8:00 AM

F3: It's all About Data: Building Blocks, Compute, Movement and Integration

F4: Highlights of Data-Converter R&D in the Past 5 Years: A Comprehensive Overview

F5: Seeing the Future: Advances in Image and Vision Sensing

F6: Evolution of the Software-Defined Vehicle: Navigating Smart Cockpits and In-Car Hardware

Short Course

8:00 AM

SC: Advances in Wireless and RF Transceiver Circuits

ISSCC 2025 Circuit Insights

(Saturday, Feb. 15, 2025, 9:00 AM – 6:00 PM)

Organizer/Moderator:
Ali Sheikholeslami, *University of Toronto, Toronto, Canada*
ISSCC Education Chair

ISSCC 2025 offers the fourth edition of its Circuit Insights on Saturday, Feb. 15, 2025, 9:00am - 6:00pm PST. As in the past three years, this event is targeting 3rd- and 4th-year undergraduate students and starting graduate students in the area of circuit design but may be of interest to new circuit design engineers as well. The event will be held in person for a small audience of 50 students (by invitation only) at the ISSCC venue at the Marriott Hotel in San Francisco, and will be recorded for later release on the SSCS/ISSCC YouTube channel.

The event consists of highlights of the past Circuit Insights and five 50-minute talks on circuit design from industry perspective. There will be will a 10-minute interactive Q&A Session at the end of each talk.

Agenda

Time	Topic
8:30 AM	Coffee
9:00 AM	**Welcoming Remarks** **Edith Beigné,** *ISSCC Conference Chair* **Bill Bowhill,** *SSCS President*
9:10 AM	**Highlights of the Past Circuit Insights** **Ali Sheikholeslami,** *University of Toronto, Toronto, Canada*
10:00 AM	**Circuit Design with Process Variation** **Roberto Maurino,** *Analog Devices, Italy*
10:50 AM	Break
11:10 AM	**Memory Circuit Design** **Dan Vimercati,** *Micron Semiconductor Inc., Folsom, CA*
12:00 PM	Networking Lunch
1:00 PM	**Circuits for Wireline Communication** **Kevin Zheng,** *AMD, San Jose, CA*
1:50 PM	**Circuits for Wireless Communication** **Hooman Darabi,** *Broadcom, Irvine, CA*
2:40 PM	Break
3:00 PM	**Circuits for Optical Communication** **Vivek Gurumoorthy,** *Marvell Technology Inc., Santa Clara, CA*
3:50 PM	Panel Discussion (with all the Speakers)
4:40 PM	Attendees Feedback/Quiz, Group Photo
5:00 PM	Ice Cream and Networking (with Speakers, SRP attendees, ISSCC ITPC Members)
6:00 PM	Conclusion

There are a total of 10 tutorials this year on 10 different topics. Each tutorial, selected through a competitive process within each subcommittee of the ISSCC, presents the basic concepts and working principles of a single topic. These tutorials are intended for non-experts, graduate students and practicing engineers who wish to explore and understand a new topic.

Sudip Shekhar
ISSCC Tutorials Chair

8:30 AM
T1: Low-Noise Current Sensing
Jens Anders
University of Stuttgart, Stuttgart, Germany

Low-noise current readouts are indispensable components in modern electronics, facilitating accurate measurement of tiny currents with the highest possible signal-to-noise ratio. They find applications in various fields, including sensor interfaces, medical devices, and environmental monitoring systems. In this tutorial, after a short motivation including some example applications and specifications, we review the basics of resistive and capacitive feedback transimpedance amplifiers, including the relevant feedback theory. We then discuss more recent implementations, including low-noise current-input ΣΔ modulators, current conveyors, and current-to-frequency converters before we conclude the tutorial with a brief summary, highlighting relevant work at ISSCC 2025.

Jens Anders received a master's degree from the University of Michigan, Ann Arbor, MI, USA, in 2005, a Dipl.-Ing. degree from the Leibniz University of Hannover in 2007, and a Ph.D. degree from EPFL in 2011. He is now a Full Professor and the Director of the Institute of Smart Sensors at the University of Stuttgart. He is also the Co-Director of the Institute for Microelectronics Stuttgart (IMS CHIPS). His research interests include integrated interface circuits with a focus on quantum sensors. Dr. Anders has authored more than 200 publications. He has served on the TPCs of ISSCC and ESSERC.

8:30 AM
T2: Fundamentals of DRAM I/O: Standards and Circuits
Hyeran Kim
Samsung Electronics, Hwaseong, South Korea

DRAM has evolved in terms of speed and capacity, with different characteristics to adjust various applications. DDR for servers or PCs, LPDDR for mobile applications, GDDR for graphics cards, and HBM for high-performance GPUs are optimized for their own applications. In particular, each DRAM I/O is introducing various technologies to double the pin speed when switching generations based on different characteristics, from signaling to equalization. We will introduce the specific circuit techniques to meet the requirements of DDR5, LPDDR5, HBM3E, and GDDR7 interfaces, which are currently undergoing a generation transition, and the basics of BER (bit-error rate) target and I/O error check in each system.

Hyeran Kim received the B.S. and M.S. degrees in information and communication engineering and the Ph.D. degree in semiconductor and display engineering from Sungkyunkwan University, Suwon-si South Korea, in 2004, 2006, and 2020, respectively. She joined Samsung Electronics, Hwaseong, South Korea, in 2006, where she has been involved in the design of dynamic random access memory (DRAM), such as GDDR and LPDDR. Her research interests include high-speed interface and clocking circuits, and the next-generation memory architecture. Dr. Kim has been serving on the Technical Program Committee for the IEEE international Solid-State Circuits Conference (ISSCC) since 2021.

8:30 AM

T3: Fundamentals of Cryo-CMOS Circuits and Systems for Quantum Computing

Fabio Sebastiano
Delft University of Technology, Delft, The Netherlands

Cryo-CMOS electronics is an enabling technology for large-scale quantum computers, which will require a cryogenic electronic interface very close to the cryogenic qubits. After reviewing the behavior of CMOS devices at cryogenic temperature and the requirements for interfacing with various qubits, this tutorial will provide an overview of state-of-the-art cryo-CMOS circuits and SoCs. We will then discuss the future challenges and the viable directions to build the electronics for future quantum computers.

Fabio Sebastiano received the B.Sc. (2003) and M.Sc. (2005) degrees in EE from the University of Pisa, the M.Sc. degree (2006) in engineering from Sant'Anna School of Advanced Studies in Pisa, and the Ph.D. degree (2011) in EE from Delft University of Technology. After being with NXP Semiconductors (2006 to 2013), he joined Delft University of Technology, where he is currently an Associate Professor interested in cryogenic electronics, quantum computing, sensor read-outs, and frequency references. Dr. Sebastiano was an IEEE Distinguished Lecturer for the Solid-State Circuits Society, and serves/had served on several TPCs (ISSCC, RFIC, IMS) and as Associate Editor of the JSSC and TVLSI. He was co-recipient of several awards, including the ISSCC 2020 Jan van Vessem Award for Outstanding European Paper.

10:30 AM

T4: Fundamental Circuits for Nanopower and Energy-Harvesting Applications

Joey Sankman
Analog Devices, Fort Collins, CO

With the rising interest in edge computing, and the addition of AI/ML functionality, nanopower circuits are in great demand to reduce the quiescent power consumption of remote sensors. Moreover, due to limited battery size, energy harvesting is used to provide more power to sensors and to extend lifetime. In this tutorial, fundamental building blocks for nanopower circuits will be covered, including startupless low-voltage references, low-frequency clocks, and LDO regulators. Energy harvesters as well as fundamental energy harvesting interface circuits will be surveyed. Attendees can expect a deep dive into fundamental and practical analog techniques to design nanopower systems.

Joey Sankman received the B.S. degree from the University of Arizona, Tucson, AZ, and Ph.D. degree from the University of Texas at Dallas, TX in electrical engineering in 2010 and 2014, respectively. At the University of Texas at Dallas, his research included energy harvesting circuits and systems as well as high-performance switch-mode power converters. He is currently an analog/power designer at Analog Devices, Principal Member of Technical Staff, working on multiphase automotive switching converters. Previously, he was an Analog R&D Engineer working on audio amplifiers, ultra-low power circuits, and radhard gate drivers at Kilby Labs, TI, Dallas, TX. He was the recipient of the U.S. National Science Foundation Graduate Research Fellowship and the 2011 Texas Instruments/Semiconductor Research Corporation Graduate Fellowship. He has authored or co-authored 20 publications in various IEEE journals and conferences.

10:30 AM

T5: Fundamentals of RF System Analysis for IC Designers

Raja Pullela
Maxlinear, Irvine, CA

This tutorial provides key insights into wireless system analysis from a circuit designer's perspective, focusing on modulation techniques, line-up analysis, and link performance optimization. Participants will explore impairments in analog and mixed-signal components-thermal noise, phase noise, spurious signals, and distortion-and their impact on system performance. The session covers critical metrics such as Signal-to-Noise Ratio (SNR), Error Vector Magnitude (EVM), Receiver Sensitivity, Blocker performance, and Transmitter out-of-band noise. We will also introduce advanced topics, such as impairment calibrations, digital pre-distortion for power amplifiers, and software-defined radio (SDR).

Raja Pullela is the Vice President of RF/Mixed-Signal IC Design at Maxlinear. He directs the development of ICs for wireless and wireline communication technologies, driving advancements in WiFi, 5G base-station radios and PAM-4 optical transceivers. Raja holds a Ph.D. in Electrical Engineering from UC Santa Barbara and brings a holistic expertise that spans the entire lifecycle of integrated circuits, from RF system definition to managing high-volume production, ensuring both innovation and practical deployment. He holds multiple patents and has contributed to the field through numerous technical publications in leading journals and conferences.

10:30 AM

T6: Front-End Circuit Design for High-Speed Optical Transceivers

Peter Ossieur
IMEC and Ghent University, Belgium

Optical transceivers form the backbone of our ICT infrastructure and are required to transport ever-growing capacities in ever-shrinking energy and density footprints. In this tutorial, CMOS and SiGe BiCMOS front-end circuits such as low-noise broadband transimpedance amplifiers, broadband drivers for modulators and lasers will be addressed, covering low-power lumped and traveling-wave implementations. Next, it will be shown how co-design of electronics and photonics can be used to optimize performance such as bandwidth, power consumption or area. Such co-design can extend beyond quantitative optimization to include shifting functionality between the optical and electronic domain.

Peter Ossieur received the M.Sc. and Ph.D. degree in electrical engineering from Ghent University, Belgium in 2000 and 2005 respectively. He is Program Manager of wireline transceivers at imec and a part-time Associate Professor at Ghent University, Faculty of Engineering and Architecture. His research focussed on high-speed electronic integrated circuit design for transceiver applications, and optical communication systems. He authored or co-authored around 200 international conference and journal publications, and holds several patents in the aforementioned areas. He has or is serving on the ISSCC and ECOC TPCs.

1:30 PM

T7: High-Speed Analog-to-Digital Converters

Vanessa Chen
Carnegie Mellon University, Pittsburgh, PA

High-speed ADCs are critical in applications spanning from wideband wireless communication to ultra-high-speed wireline and optical links, but achieving rapid operation poses unique design challenges. Beginning with fundamentals, the tutorial dives into design tradeoffs of high-speed ADC building blocks such as samplers and single-channel ADCs. Next, special attention is given to time-interleaving techniques aimed at enhancing speed, including architectural choices, impairments and calibration methodologies. Practical considerations for performance optimization and robust operation are also addressed. To conclude, emerging architectures and applications including silicon photonics, superconducting ADCs, and machine learning-enhanced approaches are discussed to illustrate their versatility in high-speed systems.

Vanessa Chen is an Assistant Professor at Carnegie Mellon University. During her doctoral studies at CMU, she conducted research on algorithm-assisted approaches to enhance energy efficiency for ultra-high-speed ADCs with on-chip real-time calibration. Prior to academia, she held positions as a circuit designer at Qualcomm and Realtek, developing self-healing RF/Mixed-signal circuits. Her current research focuses on AI-enhanced circuits and systems, including intelligent sensory interfaces, RF/mixed-signal hardware security, and ubiquitous sensing and computing systems. She has served as an Associate Editor for IEEE TCAS-I, TBioCAS, and OJCAS, and participated as a TPC member for IEEE ISSCC, VLSI, CICC, A-SSCC, and DAC.

1:30 PM

T8: Intelligent Neural Interfaces: Fundamentals and Future Directions

Mahsa Shoaran
EPFL, Geneva, Switzerland

In the past decade, there has been growing interest in developing AI-enabled neural interfaces for various neurological disorders and emerging brain-machine interface (BMI) applications. The focus has shifted from raw signal acquisition and data compression for off-body processing to intelligent systems featuring on-site signal processing, neural biomarker extraction, and AI. In this tutorial, I discuss the key characteristics, design trade-offs, and recent advances in CMOS-based systems-on-chip (SoCs) for diverse categories of intelligent neural prostheses. These categories include real-time symptom tracking and closed-loop stimulation, intelligent BMI systems for movement and communication recovery following paralysis, and beyond.

Mahsa Shoaran is currently a Tenure-Track Assistant Professor in Electrical and Micro Engineering and Neuro-X at EPFL and Director of the Integrated Neurotechnologies Laboratory. From 2017 to 2019, she was an Assistant Professor of ECE at Cornell University, following her Postdoctoral work in EE and MedE at Caltech (2015 to 2017). She received her PhD from EPFL in 2015 and her B.Sc. and M.Sc. degrees from Sharif University of Technology (2008, 2010). Dr. Shoaran is a recipient of the ERC Starting Grant (2021) and the Google AI Faculty Research Award in Machine Learning and Data Mining (2019). Her team received the IEEE SSCS-Brain Best Paper Award in 2022 for its work on NeuralTree. She was named a Rising Star in EECS at MIT in 2015. Her research focuses on low-power IC design for neural interfaces, machine-learning hardware, and neuromodulation therapies for neurological and psychiatric disorders. Dr. Shoaran serves or has served on the Technical Program Committee of the IEEE ISSCC and CICC, as an Associate Editor for IEEE TBioCAS, and on the ISSCC SRP committee.

3:30 PM

T9: Generative AI on Edge Devices: Models, Hardware and Systems

Paul Whatmough
Qualcomm, Cambridge, MA

Generative AI models have introduced unprecedented new capabilities to edge devices, everything from writing poetry to summarizing complex documents, generating incredible images and even video clips. However, this new breed of neural networks, spanning large language, vision and multi-modal models, poses numerous challenges for edge devices, stressing both compute and memory-system performance and driving active research across many disciplines. In this tutorial, I will discuss the latest Generative AI networks and the challenges they present for the hardware system, along with the latest network/hardware co-design opportunities to help close the power and performance gap for edge-device AI applications.

Paul N. Whatmough is Director of AI Research at Qualcomm Inc. and based in Cambridge, MA. He received the B.Eng. degree (Hons.) from Lancaster University, U.K., the M.Sc. degree (Hons.) from the University of Bristol, U.K., and the Ph.D. degree from University College London, U.K., in 2003, 2004, and 2012, respectively. From 2005, he was with Philips/NXP Research Labs, Redhill, U.K., researching hardware architecture and signal processing for software-defined radio. From 2008, he was with the Silicon Research and Development Group, ARM Ltd., Cambridge, U.K., working on topics, including DSP hardware accelerators, variation tolerance, and system-on-chip (SoC) supply-voltage noise. From 2015, he was a Research Associate with Harvard University, Cambridge, MA, USA. From 2017 to 2022 he led the Arm ML Research Lab, Boston, MA, USA, focusing on efficient hardware/algorithm co-design for embedded ML applications. He remains a part-time Associate with the John A. Poulson School of Engineering and Applied Sciences (SEAS), Harvard University. He coauthored the book Deep Learning for Computer Architects (Morgan & Claypool, 2017).

3:30 PM

T10: mm-Wave Oscillator Design

Jun Yin
University of Macau, Macau, China

High-performance, low-phase-noise oscillators are heavily demanded by high-throughput and high-fidelity mm-wave wireless transceivers. After briefly introducing the oscillator's performance matrix and key Figure of Merit (FoM), this tutorial will describe the reactive-load design, namely - inductors/transformers and tunable capacitors, for achieving high quality factor and illuminating the design challenge for mm-wave oscillators. It will introduce various oscillator topologies to reduce phase noise, such as Class-C and harmonic shaping. The tutorial will also cover the multi-core synchronized oscillator, which provides an opportunity for further reducing phase noise. Means to extend the tuning range of multi-core oscillators at mm-wave frequencies with the aid of mode-switching and multi-resonance techniques will also be presented.

Jun Yin received the B.Sc. (2004) and the M.Sc. (2007) degrees in Microelectronics from Peking University, Beijing, China, and the Ph.D. (2013) degree in ECE from Hong Kong University of Science and Technology (HKUST), Hong Kong, China. He is currently an Associate Professor at the State Key Laboratory of Analog and Mixed-Signal VLSI, University of Macau, Macau, China. His research areas are circuits for high-speed communications and low-power IoTs. He has authored or co-authored 1 book, 3 book chapters, and more than 90 peer-reviewed international conference and journal publications. He serves or has served on the TPCs for ISSCC, ESSERC, and A-SSCC. He was an Associate Editor of TCAS-I.

Unlocking Innovation: Circuit Techniques and New Approaches for Die-to-Die Links and the Chiplet Ecosystem

Organizers:
Zeynep Toprak Deniz, *IBM Research, Yorktown Heights, NY*
Didem Turker Melek, *Cadence Design Systems, San Jose, CA*

Co-Organizers:
Juang-Ying Chueh, *Etron Technology, Taipei, Taiwan*
Kenny Hsieh, *TSMC, Hsinchu, Taiwan*
Shidhartha Das, *Advanced Micro Devices, Cambridge, United Kingdom*
Tamer Ali, *Mediatek, Irvine, CA*

Champions:
Wei-Zen Chen, *National Yang Ming Chiao Tung University, Taiwan*
Bill Redman-White, *Top-IC, Southampton, United Kingdom*

The chiplet ecosystem and the concept of heterogeneous integration on advanced packaging are at the forefront of semiconductor technology, reflecting a paradigm shift in how high-performance chips are designed, manufactured, and integrated. Chiplet technologies promise to unlock new possibilities and address the evolving needs of diverse markets, ultimately reshaping the future of semiconductor innovation and production. This Forum will provide an in-depth examination of the current state of chiplet technology. Speakers will focus on different aspects of design for achieving important performance metrics in high density die-to-die links for chiplets. Topics will include circuit techniques for achieving ultra-low power consumption, low latency, high bandwidth density, resilience towards supply noise and crosstalk, and small area, as well as enhanced Electronic Design Automation (EDA) tools for the chiplet ecosytem.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Zeynep Toprak Deniz,** *IBM Research, Yorktown Heights, NY*
8:25 AM	**The Business of Making Chiplets and Associated Systems** **Anu Ramamurthy,** *Open Compute Project Foundation, Newbury Park, CA*
9:10 AM	**UCIe: Requirements and Innovations in Electrical Link Circuits** **Joe Wu**, *Intel, San Jose, CA*
9:55 AM	Break
10:10 AM	**Single-Ended Transceiver Design for Die-to-Die Links** **Kihwan Seong,** *Samsung Electronics, GyeongGido, Korea*
10:55 AM	**Simultaneous Bidirectional Transceivers for Low-Power Die-to-Die Links** **Ramin Farjardad,** *Eliyan, Santa Clara, CA*
11:40 AM	**uLED Parallel Optical IO for D2D Links** **Ehsan Afshari,** *University of Michigan, Ann Arbor, MI*
12:25 PM	Lunch
1:40 PM	**Chiplet EDA Tools, Chiplet Based System-Technology Co-Optimization** **Henry Sheng,** *Synopsys, San Mateo, CA*
2:25 PM	**High BW Efficient Low Power Die to Die Links** **Kevin Geary,** *Cadence, Cork, Ireland*
3:10 PM	Break
3:25 PM	**From Monolithic 2D to Heterogeneous Integration: An Advanced Packaging Technologies Landscape** **Nicolas Pantano,** *imec, Leuven, Belgium*
4:10 PM	**Design and Assembly of an Automotive-Grade Chiplet-Based System-on-Chip (SoC)** **Francois Piednoel De Normandie,** *Mercedes, Sunnyvale, CA*
4:55 PM	Closing Remarks

Wireless Communication Technology for Space Applications: From Satellite to Dish and Smartphones

Organizers:
Matteo Bassi, *Infineon Technologies, Villach, Austria*
Giuseppe Gramegna, *imec, Leuven, Belgium*

Co-Organizers:
Kuo-Ken Huang, *Everactive, San Jose, CA*
Wei Deng, *Tsinghua University, Beijing, China*
Danielle Griffith, *Texas Instruments, Dallas, TX*
Amy Whitcombe, *Intel, Santa Clara, CA*

Champions:
Jeff Walling, *Virginia Tech, Blacksburg, VA*
Jaehyouk Choi, *Seoul National University, Seoul, Korea*

This forum brings together leading researchers and industry experts to explore the cutting-edge developments in satellite communication systems. Speakers will engage in discussions on enabling technologies and the challenges associated with designing electronics for aerospace applications, with an emphasis on the emerging non-terrestrial mobile telecommunication systems. Presentations will highlight recent advancements in wireless transceivers employed in satellites, mobile devices, and ground stations. The selected topics will delve into the complete stack of innovations required for consumer, ground and satellite electronics, encompassing system-level challenges, computational architectures, transistor-level circuit implementations, and radiation-tolerant designs.

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Matteo Bassi,** *Infineon Technologies, Villach, Austria*
8:25 AM	**5G NTN Technology for Direct Satellite Access: From Smart Phone to Automotive** **I-Kang Fu**, *Mediatek, Hsinchu, Taiwan*
9:15 AM	**High Level RF Requirements for Commercial Space Systems** **Will Caven,** *Maxar Technologies, San Jose, CA*
10:05 AM	Break
10:20 AM	**CMOS System-on-Chip Instruments for Exploring Earth, the Solar System and Space** **Adrian J. Tang,** *NASA Jet Propulsion Laboratory, Pasadena, CA*
11:10 AM	**European Satellite Constellation to User Terminals: From System to Silicon** **Pierre Busson,** *ST Microelectronics, Grenoble, France*
12:00 PM	Lunch
1:20 PM	**Enabling the Next Era of Space-Based Cyber-Physical Systems Applications with Ultra-Energy-Efficient, General-Purpose Computing Hardware** **Brandon Lucia,** *Efficient Computer & Carnegie Mellon University, Pittsburgh, PA*
2:10 PM	**Foldable Phased-Array Transceivers for Satellite Communications** **Kenichi Okada,** *Institute of Science Tokyo, Tokyo, Japan*
3:00 PM	Break
3:15 PM	**Heterogenous Integration Technologies Suitable for SatCom Applications** **C.P. Hung,** *ASE Global, Kaohsiung, Taiwan*
4:05 PM	**Radiation-Hardened Memories for Space Applications** **Helmut M.N. Puchner,** *Infineon Technologies, San Jose, CA*
4:55 PM	Closing Remarks

Bingo Networking Event
(Open to all Attendees)
4:00 - 6:00 PM

Women in Circuits (WiC) together with ISSCC will be holding a networking and mentoring session on Sunday afternoon. Distinguished panelists, WiC members, and other participants will play getting-to-know-you bingo to promote engagement between various members of the community. This will give participants the chance to network and mingle with people across a spectrum of seniority in the field in a casual setting. This event is open to all ISSCC attendees and the public.

EE1: Student Research Preview (SRP) 8:00 PM

The Student Research Preview (SRP) will highlight selected student research projects in progress. The SRP consists of 24 sixty-second presentations followed by a Poster Session, by graduate students from around the world, which have been selected on the basis of a short submission concerning their on-going research. Selection is based on the technical quality and innovation of the work. This year, the SRP will be presented in three theme sections: 1) Power and Analog, 2) ML, Cryogenic and Ising Machine, and 3) Data Communications and Frequency Generation.

The SRP will include an inspirational lecture by Professor Jan Rabaey (UC Berkeley). SRP begins at 8:00 pm on Sunday, February 16th. It is open to all ISSCC registrants.

SRP Organizing Committee

Co-Chair:	**Jerald Yoo**, *Seoul National University, Korea*
Co-Chair:	**Mondira (Mandy) Pant**, *Intel, MA*
Advisor:	**Anantha Chandrakasan**, *Massachusetts Institute of Technology, MA*
Advisor:	**Jan Van der Spiegel**, *University of Pennsylvania, Philadelphia, PA*
Media/Publications:	**Laura Fujino**, *University of Toronto, Toronto, Canada*
A/V:	**Trudy Stetzler**, *Halliburton, Houston, TX*

Committee Members

Utsav Banerjee
IISC, India

Po-Hung Chen
National Yang Ming Chiao Tung University Taiwan

Woo-Seok Choi
Seoul National University Korea

Sijun Du
Delft University of Technology The Netherlands

Antoine Frappé
University of Lille, France

Hao Gao
Eindhoven University of Technology The Netherlands

Preet Garcha
Texas Instruments, TX

Takuji Miki
Kobe University, Japan

Matthias Kuhl
University of Freiburg Germany

Jaydeep Kulkarni
University of Texas, at Austin TX

Jiamin Li
Southern University of Science and Technology China

Xilin Liu
University of Toronto Canada

Noriyuki Miura
Osaka University, Japan

Phillip Nadeau
Analog Devices, MA

Mondira Pant
Intel, MA

Nandish Mehta
Nvidia, CA

Chutham Sawigun
imec, Belgium

Hyunjoo Jenny Lee
KAIST, Korea

Mahsa Shoaran
EPFL, Switzerland

Bongjin Kim
UCSB

Zeynep Deniz
IBM Research, NY

Filip Tavernier
KU Leuven, Belgium

Hsiao-Chin Chen
National Taiwan University of Science and Technology Taiwan

Lita Yang
Meta

Kyuho Jason Lee
UNIST, Korea

Jerald Yoo
Seoul National University Korea

Lian Zhang
Apple, CA

Plenary Session — Invited Papers

Chair: **Edith Beigné,** *Meta, Menlo Park, CA*
ISSCC Conference Chair

Associate Chair: **Thomas Burd,** *Advanced Micro Devices, Santa Clara, CA*
ISSCC International Technical-Program Chair

FORMAL OPENING OF THE CONFERENCE **8:30 AM**

1.1 AI Era Innovation Matrix — 8:50 AM

Navid Shahriari, *Senior Vice President,*
Foundry Technology Development
Intel, Chandler, AZ

AI holds transformative potential for humanity, enhancing our ability to solve complex problems with speed and accuracy, and unlocking new realms of innovation and understanding. The lightning-fast progression of AI, unprecedented in history, necessitates rapid advancements at a system level, from low-power and edge-AI devices to cloud-based computing, and in the communication networks that connect them. This need for rapid AI system scaling is driving the innovation frontier in silicon, packaging, architecture, and software. This paper describes a matrix of technologies that empowers the industry to achieve remarkable progress at every level, from chips to systems.

1.2 From Chips to Thoughts: Building Physical Intelligence into Robotic Systems — 9:20 AM

Daniela Rus, *Massachusetts Institute of Technology, Director, CSAIL & Andrew (1956) and Erna Viterbi Professor, Cambridge, MA*

In today's robot revolution, a record 3.1 million robots are now working in factories, doing everything from assembling computers to packing goods and monitoring air quality and performance. A far greater number of smart machines impact our lives in countless other ways—improving the precision of surgeons, cleaning our homes, extending our reach to distant worlds—and we are on the cusp of even more exciting opportunities. Future machines, enabled by recent advances in AI, will come in diverse forms and materials, embodying a new level of physical intelligence. Physical Intelligence is achieved when the power of AI to understand text, images, signals, and other information is used to make physical machines such as robots intelligent. However, a critical challenge remains: balancing the capabilities of AI with sustainable energy usage. To achieve effective physical intelligence, we need energy-efficient AI systems that can run reliably on robots, sensors, and other edge devices. In this paper I will discuss the energy challenges of transformer-based foundational AI models, I will introduce several state space models, and explain how they achieve energy efficiency, and how state-space models enable physical intelligence.

ISSCC, SSCS, IEEE AWARD PRESENTATIONS **9:50 AM**

BREAK **10:15 AM**

1.3 AI Revolution Driven by Memory Technology Innovation — 10:45 AM

Jaihyuk Song, *Corporate President & CTO, Device Solutions, Samsung Electronics, Hwaseong, South Korea*

The recent AI revolution, spearheaded by Large Language Models (LLMs), demands substantial computing resources and corresponding memory solutions. However, unlike processors that can leverage advancements in fabrication processes, memory devices are increasingly struggling to meet the high bandwidth, large capacity, and power efficiency requirements of AI systems. This paper analyzes the requirements and limitations of systems in the AI era, categorizing application-specific memory needs in terms of performance, power, and capacity. We introduce performance-centric solutions such as HBM (High Bandwidth Memory) and PIM (Processing-In-Memory) technologies, energy-efficient solutions including custom HBM and LPW (LPDDR Wide-IO) memory, and capacity-focused solutions like SSD (Solid-State Drives) and CXL (Compute Express Link) Memories. Additionally, we discuss how continuous scaling of DRAM and NAND Flash processes, as well as 3D-packaging technologies, can address the trade-offs among performance, power, and capacity more effectively. Finally, the importance of software technologies in optimizing the utilization of these increasingly specialized memory solutions is emphasized, along with a discussion of the enabling core technologies for each solution. To meet the high demands of AI systems, the ongoing advancement of existing memory devices and the development of new memory solutions will play crucial roles. These efforts will support the advancement of AI technologies and contribute to human society.

1.4 The Crucial Role of Semiconductors in the Software-Defined Vehicle — 11:15 AM

Peter Schiefer, *President & CEO, Automotive Division, Infineon Technologies, Munich, Germany*

The automotive industry is undergoing a significant transformation, driven by the rise of software-defined vehicles (SDVs). Semiconductors will play a pivotal role in enabling this transition, powering the complex systems that underpin the features and functions of modern cars. This paper explores the key trends driving the growth of the automotive semiconductor market, including green mobility, autonomous driving, and smarter cars. It delves into the challenges and opportunities associated with the development of SDVs, highlighting the importance of advanced microelectronics, artificial intelligence, and secure communication solutions. The paper concludes by emphasizing the crucial role of semiconductors in shaping the future of mobility. By addressing the challenges and embracing the opportunities presented by SDVs and AI, the automotive industry can create a more sustainable and innovative future.

PRESENTATION TO PLENARY SPEAKERS — 11:45 AM

CONCLUSION — 11:50 AM

Processors

Session Chair: Jie Gu, *Northwestern University, Evanston, IL*
Session Co-Chair: *Nathaniel Pinckney, Nvidia, Austin, TX*

1:30 PM

2.1 "Zen 5": The AMD High-Performance 4nm x86-64 Microprocessor Core

T. Singh[1], S. Rangarajan[1], S. Southard[1], C. Henrion[2], A. Schaefer[1], S. Oliver[1], B. Johnson[2], S. B. Tower[1], K. Hoover[1], D. John[1], T. Antoniadis[1], S. Lakshman[1], V. Mittal[1], B. Kasprzyk[1], R. McCoy[1], K. Mohlman[1], A. Mohan[1], H-H. Wong[3], D. Lieu[3], R. Schreiber[1], S. Singh[4], N. Lance[2], D. Prudich[2], J. Coppin[2], T. Jackson[2], A. Karegar[2], R. Miller[2], S. Balagangadharan[5], J. Pistole[3], W. Li[3], M. McCabe[3]

[1]AMD, Austin, TX, [2]AMD, Fort Collins, CO
[3]AMD, Santa Clara, CA; [4]AMD, Markham, Canada
[5]AMD, Bangalore, India

1:55 PM

2.2 IBM Telum II: Next Generation 5.5GHz Microprocessor with On-Die Data Processing Unit and Improved AI Accelerator

G. Strevig[1], C. Berry[2], R. Rao[3], N. Jungmann[4], M. Sperling[2], M. Becht[2], E. Herkel[5], M. Pflanz[6], P. Meaney[2], M. Romain[2], M. Cichanowski[1], A. Venton[1], D. Wolpert[2], E. Kachir[4], L. Hopkins[2], T. Bubb[2], A. Arp[5], D. Kiss[5], S. Büchsenstein[5], M. Wood[2], M. Spear[1], R. Sonnelitter[2], R. Joshi[6]

[1]IBM Systems, Austin, TX; [2]IBM Systems, Poughkeepsie, NY
[3]IBM Systems, Bangalore, India; [4]IBM Systems, Tel Aviv, Israel
[5]IBM Systems, Böblingen, Germany; [6]IBM Research, Yorktown Heights, NY

2:20 PM

2.3 Granite Rapids-D: Intel Xeon 6 SoC for vRAN, Edge, Networking, and Storage

R. R. Varada[1], R. Krishnan[2], A. Subramonia[2], R. Chandran[2], K. Chakravarthy[2], U. D. Desai[2], S. Limaye[2], P. Puri[2], D. R. Mulvihill[3], M. Bichan[4], M. Koolhaas[4], V. Ramachandran[5], S. Kondle[5]

[1]Intel, Santa Clara, CA; [2]Intel, Bengaluru, India
[3]Intel, Fort Collins, CO; [4]Intel, Toronto, Canada
[5]Intel, Chandler, AZ

2:45 PM

2.4 A 300MB SRAM, 20Tb/s Bandwidth Scalable Heterogenous 2.5D System Inferencing Simultaneous Streams Across 20 Chiplets with Workload-Dependent Configurations

S. Rangachar Srinivasa[1], D. Kurian[1], P. Aseron[1], P. Budhkar[1], A. Radhakrishnan[1], A. Cardenas Lopez[1], J. Sundaram[1], V. Honkote[1], L. Azarenkov[1], D. Lake[1], J. Timbadiya[2], M. Moiseev[1], B. Perez Esparza[3], R. Kalim[1], E. Ramirez Lozano[3], M. Bhartiya[2], S. Kabisthalam Muthukumar[2], S. Yada[1], S. Kadavakollu[2], S. Chhabra[2], K. Prasad Sahu[2], J. Greensky[1], X. Brun[4], E. Juarez Hernandez[3], R. Munoz[4], T. Thomas[1], S. Liff[4], V. De[1], A. Srinivasan[1], T. Karnik[1]

[1]Intel, Hillsboro, OR; [2]Intel, Bangalore, India
[3]Intel, Guadalajara, Mexico; [4]Intel, Chandler, AZ

3:00 PM

2.5 DS1 A 16nm 5.7TOPS CNN Processor Supporting Bi-Directional FPN for Small-Object Detection on High-Resolution Videos

Y-C. Ding[1], C-Y. Chang[1], C-Y. Lin[1], H-Y. Tsai[1], H-J. Tu[1], K-F. Chang[1], Y-C. Su[1], T-H. Hsieh[1], Y-K. Jian[1], W-C. Chen[2], N-S. Chang[2], C-P. Lin[2], C-S. Chen[2], C-T. Huang[1]

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

Break 3:15 PM

3:35 PM

2.6 DS1 1.78mJ/Frame 373fps 3D GS Processor Based on Shape-Aware Hybrid Architecture Using Earlier Computation Skipping and Gaussian Cache Scheduler

X. Feng, H. Wang*, C. Tang, T. Wu, H. Yang, Y. Liu*

Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

4:00 PM

2.7 DS1 IRIS: An 8.55mJ/frame Spatial Computing SoC for Interactable Rendering and Surface-Aware Modeling with 3D Gaussian Splatting

S. Song, S. Kim, W. Park, J. Park, S. An, G. Park, M. Kim, H-J. Yoo

KAIST, Daejeon, Korea

4:25 PM

2.8 A 210fps Image Signal Processor for 4K Ultra HD True Video Super Resolution

Y-S. Lin[1], J. Nishimura[2], C-H. Yang[1]

[1]National Taiwan University, Taipei, Taiwan
[2]Google, Mountain View, CA

4:50 PM

2.9 DS1 STEP: An 8K-60fps Space-Time Resolution-Enhancement Neural-Network Processor for Next-Generation Display and Streaming

K-P. Lin[1], T. Wu[1], C-P. Lin[1], P-W. Chen[1], Z-J. Zhang[1], W-S. Khwa[2], M-F. Chang[2], C-T. Huang[1]

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC Corporate Research, Hsinchu, Taiwan

5:15 PM

2.10 A 0.52mJ/Frame 107fps Super-Resolution Processor Exploiting Pseudo-FP6 Sparsity for Mobile Applications

X. Duan, X. Shi, Z. Zhou, Z. Shu, Y. Rong, Y. Chen, Z. Yang, M. Li, J. Han

Fudan University, Shanghai, China

Conclusion 5:30 PM

Amplifiers and Analog Front-Ends

Session Chair: Giulio Ricotti, *STMicroelectronics, Cornaredo, Italy*
Session Co-Chair: Jiawei Xu, *Fudan University, Shanghai, China*

1:30 PM

3.1 A 121.3dB-DR, 115dB-PSNR, Digital-Input Capacitive-Feedback Class-D Audio Amplifier with Double-Sided Voltage-Boosting (DSVB) Modulation

J-W. Cyue, T-H. Kuo
National Cheng Kung University, Tainan, Taiwan

1:55 PM

3.2 A 36V Current-Balancing Instrumentation Amplifier with ±24V Input Range, 5.6MHz BW, and 140dB CMRR at All Gain Settings

S. Ye, M. Jiang, J. Wang, S. Zhang, P. Cao, Z. Hong, J. Xu
Fudan University, Shanghai, China

2:20 PM

3.3 A Passive Switched-Capacitor-Based Multimode Amplifier with a Logarithmic Conformity Error of 0.75% from -25 to 200°C

H. Siemssen[1], R. Nowosielski[2], H. Borchardt[2], J. Mueller[2], B. Wicht[1]
[1]Leibniz University Hannover, Hannover, Germany
[2]Baker Hughes, Celle, Germany

2:45 PM

3.4 A CMOS Operational Amplifier Achieving ±5.8μV 3σ Offset and ±88nV/°C 3σ Offset Drift Using an On-Chip Heater-Based Self-Trimming Technique

A. Zhang[1], M. Zhan[1], M. Chen[2], Y. Zhong[1], L. Jie[1], N. Sun[1], Q. Fan[2]
[1]Tsinghua University, Beijing, China
[2]Delft University of Technology, Delft, The Netherlands

Break 3:10 PM

Analog Techniques

Session Chair: Giulio Ricotti, *STMicroelectronics, Cornaredo, Italy*
Session Co-Chair: Jiawei Xu, *Fudan University, Shanghai, China*

3:35 PM

4.1 A 12.8GS/s Sub-Sampling ADC Front-End with 38GHz Input Bandwidth and >39dB SNDR for 1 to 32GHz in 22nm FDSOI

J. Heel[1], H. S. Bindra[1], S. Louwsma[2], A. Dezzani[3], B. Nauta[1]

[1]University of Twente, Enschede, The Netherlands
[2]Teledyne DALSA Semiconductors, Enschede, The Netherlands
[3]Teledyne e2v, Grenoble, France

4:00 PM

4.2 DS1 A 1.8-to-3.0GHz Fully Integrated All-In-One CMOS Frequency Management Module Achieving -47/+42ppm Inaccuracy from -40 to 95°C and -150/+70ppm After Accelerated Aging

R. Huo[1], T. Zhang[1], W. Jie[1], Y. Zheng[1], D. Li[1], L. Gao[2], Y. Zhao[1], H. Jiang[1], Y. Li[1], P. Mercier[3], H. Wang[1]

[1]Shanghai Jiao Tong University, Shanghai, China
[2]South China University of Technology, Guanzhou, China
[3]University of California, San Diego, CA

4:25 PM

4.3 DS1 A 0.36nW, 820µm², 32kHz Conduction-Angle-Adaptive Crystal Oscillator in 28nm CMOS for Real-Time Clock Applications

P. Wang[1], M. Wang*[1], G. Dai[1], Y. Cao[1,2], S. Pan[2], Y. Zhang[1]*

[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

4:50 PM

4.4 A 0.36nW/0.9V 32kHz Crystal Oscillator Using Analog Regulation for Cross-Current Avoidance

T. Chlan, M. Dietl, R. Brederlow

Technical University Munich, Munich, Germany

5:05 PM

4.5 A 0.4µW/MHz Reference-Replication-Based RC Oscillator with Path-Delay and Comparator-Offset Cancellation Achieving 9.83ppm/°C from -40 to 125°C

Y. Liu[1], Z. Zhu[1], X. Yang[1], R. Bao[1], Z. Zhang[2], H. Zhang[1], J. Liu[1], Z. Wang[1], M. Zhang[3], N. Yan[4], J. Yin[2], P-I. Mak[2], S. Yang[1]

[1]University of Electronic Science and Technology of China, Chengdu, China
[2]University of Macau, Macau, China
[3]M-CHIP, Chengdu, China
[4]Fudan University, Shanghai, China

5:20 PM

4.6 A 0.8V, 31ppm/°C, -40dB DC-to-GHz Power-Supply-Rejection Standard-V_{th} Core-MOS-Only Voltage Reference with a 294µm² Area

B-S. Lien, S-L. Liu*, W-L. Lai, Y-C. Lu, Y-C. Peng, K-H. Hsieh*

TSMC, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

Conclusion 5:35 PM

Front-End Circuits for High-Performance Transceivers

Session Chair: Henrik Sjoland, *Lund University, Ericsson Research, Lund, Sweden*
Session Co-Chair: Hongtao Xu, *Fudan University, Shanghai, China*

1:30 PM

5.1 A GaN SLCG-Doherty-Continuum Power Amplifier Achieving >38% 6dB Back-Off Efficiency over 1.35 to 7.6GHz

G. Lv[1], W. Chen[1], X. Chen[1], F. Huang[2], Z. Feng[1]

[1]Tsinghua University, Beijing, China
[2]Gaxtrem Technology, Beijing, China

1:55 PM

5.2 Spatial-Temporal Direct-Digital Beamforming Power Amplifier with Enhanced Back-Off Efficiency in a 24GHz Phased Array

Y. Zhao[1], Y. Song[1], W. Gu[1], S. Yu[1], Z. Yu[2], Y. Han[1], X. Zhu[3], X. Lu[1]

[1]Shanghai Jiao Tong University, Shanghai, China
[2]University of Pennsylvania, Philadelphia, PA
[3]SGR Semiconductors, Shanghai, China

2:20 PM

5.3 A 56-to-64GHz Linear Power Amplifier with 30.2dBm P_{sat} and 23.5% PAE_{peak} Using Scalable Matched-Zone-Expanding Radial Power Combining with EM-Loss Reduction in 40nm Bulk CMOS

D. Tang, B. Yang, A. Han, X. Luo

University of Electronic Science and Technology of China, Chengdu, China

2:45 PM

5.4 A 22nm FDSOI CMOS-Based Compact 3-Stack Doherty Power Amplifier with a Stacked OPA-Based Bias Scheme Achieving >16.5dBm P_{avg} for 5G FR2 Applications

J. Lee, H. Oh, S. Baek, S. Park, D. Lee, S. Jeon, T. Kim, J. Jung, S-G. Yang

Samsung Electronics, Seoul, Korea

3:00 PM

5.5 An Ultra-Compact Wideband Load-Insensitive Complex-Cascode LC-Neutralized Power Amplifier for 4:1-VSWR-Resilient Operations in Large-Scale Phased Arrays

M. Eleraky[1], T-Y. Huang[1,2], H. Wang[1]

[1]ETH Zürich, Zürich, Switzerland
[2]ARGUS SPACE AG, Zurich, Switzerland

Break 3:15 PM
3:35 PM

5.6 A Power-Efficient CORDIC-less Digital Polar Transmitter Using 1b DSM-Based PA Supporting 256-QAM

Y. Zhang, Z. Liu, D. Li, M. Tang, Y. Zhang, H. Huang, D. Xu, W. Madany, A. A. Fadila, W. Wang, Y. Xiong, D. Zhang, G. P. Kusuma, H. Sakai, K. Kunihiro, A. Shirane, K. Okada

Institute of Science Tokyo, Tokyo, Japan

4:00 PM

5.7 A 4.7GHz, 27.7dBm P_{out}, 37.8% PAE, 5.8° AM-PM Distortion Polar SCPA Using In-Cell Fast Slope-to-Phase Self-Calibration and Asymmetrical 4-to-1 Differential Power-Combining Transformer

H. Tang, B. Yang, X. Luo

University of Electronic Science and Technology of China, Chengdu, China

4:25 PM

5.8 A 20W CMOS/LDMOS All-Digital Transmitter with Dynamic Retiming and Glitch-Free Phase Mapper, Achieving 68%/62% Peak Drain/System Efficiency

D. P. N. Mul[1], R. J. Bootsman[1], M. Beikmirza[1], O. El Boustani[1], Y. Shen[1], D. Maassen[2], B. van Velzen[2], M. Rousstia[2], R. Koster[2], J. R. Gajadharsing[2], T. Fritzsch[3], M. Alavi[1], L. C. De Vreede[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Ampleon, Nijmegen, The Netherlands
[3]Fraunhofer IZM, Berlin, Germany

4:50 PM

5.9 A 21-to-31GHz DPD-less Quadrature RFDAC with Invariant Impedance and Scalable LO Leakage

H. J. Qian, W. Qin, C. Qiu, Y. Yang

Xidian University, Xi'an, China

5:05 PM

5.10 A 3.5mW mm-Wave Low-Noise Active Bandpass Filter Employing an All-Passive Interferer-Cancellation Feedforward Path

A. G. Gadelkarim, P. Mercier

University of California, San Diego, CA

5:20 PM

5.11 A Blocker-Tolerant mm-Wave Low-Noise Amplifier Utilizing Doherty Active Load Modulation for Linearity Enhancement

H. Yu, L. Liu, S. Li

University of Texas, Austin, TX

Conclusion 5:35 PM

Imagers and Displays

Session Chair: Leonardo Gasparini, *Fondazione Bruno Kessler, Trento, Italy*
Session Co-Chair: Hyung-Min Lee, *Korea University, Seoul, Korea*

1:30 PM

6.1 A 3-Stacked Hybrid-Shutter CMOS Image Sensor with Switchable 1.2µm-Pitch 50Mpixel Rolling Shutter and 2.4µm-Pitch 12.5Mpixel Global Shutter Modes for Mobile Applications

DS1

H. Shim, S-S. Kim, M-W. Seo, S. Park, H. Kwon, Y. Kim, S. Lee, S. Park, D. Bae, S. G. Koo, M. Ito, J-H. Jeon, S. Yoon, S-J. Byun, S. Kim, K. Kim, G. Cho, J. Lee, T. Kim, S. Jun, J-K. Lee, C-R. Moon, J. Song

Samsung Electronics, Hwaseong, Korea

1:55 PM

6.2 An Asynchronous 160×90 Flash LiDAR Sensor with Dynamic Frame Rates of 5 to 250fps Based on Pixelwise ToF Validation via a Background-Light-Adaptive Threshold

S. Park[1,2], S-H. Han[1], J. Kim[1], J. Kang[1], J-H. Chun[2,3], J. Choi[2,3], S-J. Kim[4]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea
[2]SolidVue, Seongnam, Korea
[3]Sungkyunkwan University, Suwon, Korea
[4]Sogang University, Seoul, Korea

2:20 PM

6.3 SPAD Flash LiDAR with Chopped Analog Counter for 76m Range and 120klx Background Light

H-S. Choi[1,2], I. Park[1,3], B. Park[4], D. Cho[1,5], M-J. Lee[1], Y. Chae[1,3]

[1]Yonsei University, Seoul, Korea
[2]Korea Institute of Science and Technology, Seoul, Korea
[3]XO Semiconductor, Seoul, Korea
[4]Myongji University, Yongin, Korea
[5]Samsung Electronics, Hwasung, Korea

2:45 PM

6.4 A 400×400 3.24µm 117dB-Dynamic-Range 3-Layer Stacked Digital Pixel Sensor

T-H. Tsai[1], K-H. Chang[2], A. Berkovich[1], R. Capoccia[3], S. Chen[1], Z. Wang[4], C. Liu[1], Y-H. Lin[2], S-Y. Lai[2], H-M. Hsu[2], H. Abe[5], K. Mori[5], H. Fukuhara[5], C-H. Lin[2], T. Isozaki[5], W-C. Li[2], W-F. Chou[2], M. Uno[5], R. Ikeno[5], M. Nagamatsu[5], G. Yang[2], S-G. Wuu[2], L. Bainbridge[6]

[1]Meta, Redmond, WA
[2]Brillnics, Hsinchu, Taiwan
[3]Meta, Zürich, Switzerland
[4]Meta, Burlingame, CA
[5]Brillnics, Tokyo, Japan
[6]Sesame AI, San Francisco, CA

Break 3:10 PM

3:35 PM

6.5 A 25.2Mpixel 120frames/s Full-Frame Global-Shutter CMOS Image Sensor with Pixel-Parallel ADC

T. Kainuma, R. Wakamatsu, K. Wada, T. Takeda, S. Ueyama, H. Suto, T. Miura, K. Uemura, M. Kimura, M. Sakakibara, Y. Oike

Sony Semiconductor Solutions, Atsugi, Japan

4:00 PM

6.6 A 320×256 6.9mW 2.2mK-NETD 120.4dB-DR LW-IRFPA with Pixel-Paralleled Light-Driven 20b Current-to-Phase ADC

Y. Zhuo[1], H. Lu[2], D. Ma[3], Z. Zhou[1], L. Shen[1], Y. Zhang[1], Z. Chen[1], X. Cao[1], Y. Cai[1], N. Li[2,3], W. Lu[1]

[1]Peking University, Beijing, China
[2]University of Chinese Academy of Sciences, Hangzhou, China
[3]Shanghai Institute of Technical Physics Chinese Academy of Sciences, Shanghai, China

4:25 PM

6.7 A 10b Source-Driver IC with All-Channel Automatic Offset Calibration and Slew-Rate-Enhanced Amplifier Achieving 2273μm²/Channel and 1.9mV DVO for 6285-PPI OLED-on-Silicon Displays

J. Oh, W. Yoo*, D-K. Lee, J-S. Kim*

Hanyang University, Ansan, Korea
*Equally Credited Authors (ECAs)

4:50 PM

6.8 A Real-Time Pixel-Compensated Source-Driver IC with Dual-Slope Error Detection and Multi-Channel Time-Multiplexing Compensator for Compact OLED Displays

J. Ahn, S. H. Choi, J. Y. An, M. Um, H-M. Lee

Korea University, Seoul, Korea

5:05 PM

6.9 A Compact 10b Source Driver IC with Delta-Sigma Pulse Width Modulation for Low-Voltage Digital Interpolation Achieving 1884μm²/Channel

J. Y. An[1,2], S. H. Choi[1], J. Ahn[1], S. Baek[2], Y. Kim[2], S-W. Kim[2], J-Y. Lee[2], Y-K. Choi[1], H-M. Lee[1]

[1]Korea University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea

5:20 PM

6.10 A 10.5mW Automotive Touch AFE IC Featuring Radiated EMI Reduction Based on Pipelined Dual-Frequency Modulation and Sine² Waveform Shaping for CISPR 25 Class 5 Compliance

S. Moon[1], J. Choi[1,2], J-E. Park[1]

[1]Sungkyunkwan University, Suwon, Korea
[2]Samsung Electronics, Hwaseong, Korea

Conclusion 5:35 PM

Ultra-High-Speed Wireline

Session Chair: Hyo Gyuem Rhew, *Samsung, Gyeonggi, Korea*
Session Co-Chair: Jay Im, *AMD, San Jose, CA*

1:30 PM

7.1 A 212.5Gb/s DSP-Based PAM-4 Transceiver with 50dB Loss Compensation for Large AI System Interconnects in 4nm FinFET

E-H. Chen[*1], *H. Park*[*2], *M. Abdullatif*[*2], *M. Gandara*[1], *A. ElShater*[1], *A. Khashaba*[1], *S-H. Huang*[2], *T-B. Liu*[2], *A. Atharav*[1], *J. Lee*[1], *Q. Nehal*[1], *M. Megahed*[1], *Y. Chun*[1], *C-E. Shieh*[2], *V. Jolly*[1], *S. Kwon*[1], *H-T. Chien*[2], *K-C. Wu*[2], *C-E. Liu*[2], *P. Yan*[1], *P-J. Li*[2], *C-H. Chen*[2], *T-S. Lin*[2], *P-C. Liu*[2], *T. Ali*[1]

[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Irvine, CA
*Equally Credited Authors (ECAs)

1:55 PM

7.2 DS1 A 2.2pJ/b 212.5Gb/s PAM-4 Transceiver with >46dB Reach in 5nm FinFET

A. Mostafa[1], *A. Hassan*[1], *A. Hsu*[2], *A. Singh*[3], *C-H. Wu*[4], *C-R. Yang*[1], *D. Prabakaran*[3], *D. Storaska*[5], *D. Zhou*[1], *D. Visani*[1], *E. Hsiao*[1], *F. Chu*[1], *F. Khan*[1], *F. Lu*[1], *G. Cui*[1], *G. Wang*[1], *J. Natonio*[5], *J. Deng*[1], *J. Ding*[1], *J. Guo*[1], *J. Gu*[1], *J. Zang*[1], *L. Jiang*[1], *K. Chang*[1], *K-M. Lu*[4], *M. Hasan*[1], *M. Kelly*[6], *M. H. Kashani*[2], *M. Gambhir*[1], *M. R. Patoju*[3], *M. Singh*[1], *M. Shannon*[5], *M. Yang*[1], *P. Liu*[1], *P. Ramakrishna*[3], *R. Chen*[4], *R. Ho*[7], *S. N. Shahi*[8], *S. Sivakumar*[1], *S. Xu*[7], *X. Yang*[1], *X. Han*[1], *Y-P. Su*[4], *Z. Adal*[1], *Z. Guo*[1], *Z. Li*[1], *Z. Yu*[1], *Z. Yan*[1], *H. Wang*[1], *K. Chang*[1]

[1]Marvell, Santa Clara, CA
[2]Marvell, Toronto, Canada
[3]Marvell, Bangalore, India
[4]Marvell, Zhubei, Taiwan
[5]Marvell, Fishkill, NY
[6]Marvell, Massachusetts, MA
[7]Marvell, Burlington, VT
[8]Marvell, Kanata, Canada

2:20 PM

7.3 A 1.11pJ/b 224Gb/s XSR Receiver with Slice-Based CTLE and PI-Based Clock Generator in 12nm CMOS

B. Ye[1,2], *T. Ye*[1], *T. Zhong*[1], *Z. Huang*[1], *L. Shen*[1], *B. Zhang*[1], *D. Yu*[1], *Y. He*[1], *W. Gai*[1,3]

[1]Peking University, Beijing, China
[2]East China Normal University, Shanghai, China
[3]Beijing Advanced Innovation Center for Integrated Circuits, Beijing, China

2:45 PM

7.4 DS1 A 112Gb/s DSP-Based PAM-4 Receiver with an LC-Resonator-Based CTLE for >52dB Loss Compensation in 4nm FinFET

H. Park[*1], *Q. Nehal*[*1], *M. Gandara*[1], *A. Atharav*[1], *J. Lee*[1], *J. Li*[2], *T. Ali*[1]

[1]MediaTek, Irvine, CA
[2]MediaTek, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

Break 3:10 PM

3:35 PM

7.5 A 353mW 112Gb/s Discrete Multitone Wireline Receiver Datapath with Time-Based ADC in 5nm FinFET

J. Lee[1,2], P-A. Francese[2], M. Brändli[2], T. Morf[2], M. Kossel[2], S. Jang[1], G. Kim[1]

[1]Daegu Gyeongbuk Institute of Science and Technology, Daegu, Korea
[2]IBM Research Europe, Rüschlikon, Switzerland

4:00 PM

7.6 DS1 A 2.06pJ/b 106.25Gb/s PAM-4 Receiver with 3-Tap FFE and 1-Tap Speculative DFE in 28nm CMOS

Y-P. Lin, Y-C. Jao, W-H. Hsieh, P-J. Peng

National Tsing Hua University, Hsinchu, Taiwan

4:25 PM

7.7 A 50Gb/s Burst-Mode NRZ Receiver with 5-Tap FFE, 7-Tap DFE and 15ns Lock Time in 28nm CMOS for Symmetric 50G-PON

B. Zhang[1,2], T. Ye*[1], S. Ma[3], T. Zhong[1], X. Liu[1], F. Zhang[3], B. Ye[4], D. Li[3], W. Gai[1,2]*

[1]Peking University, Beijing, China
[2]Beijing Advanced Innovation Center for Integrated Circuits, Beijing, China
[3]Xi'an JiaoTong University, Xi'an, China
[4]East China Normal University, Shanghai, China
*Equally Credited Authors (ECAs)

4:50 PM

7.8 A Reference-less CDR Using SAR-Based Frequency-Acquisition Technique Achieving 55ns Constant Band-Searching Time and up to 63.64Gb/s/μs Acquisition Speed

X. Zhao, Y. Zhang, H. Chang, Y. Dong, C. Han, Z. Yang, Z. Dong, R. Zhou, S. Liu, Z. Zhu

Xidian University, Xi'an, China

5:05 PM

7.9 A 60Gb/s NRZ Burst-Mode CDR with Cross-Injection Locking and Flash Phase Detector Achieving 0.13ns Reconfiguration Time in 28nm CMOS

S. Wei, R. Tang, C. Cao, Y. Su, K. Wang, Z. Ye, H. Sun, K. Fu, X. Gui

Xi'an JiaoTong University, Xi'an, China

5:20 PM

7.10 An 8-to-28GHz 8-Phase Clock Generator Using Dual-Feedback Ring Oscillator in 28nm CMOS

Y. Tian, J. Gu, W. He, S. Liu, H. Xu, N. Yan

Fudan University, Shanghai, China

Conclusion 5:35 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 17th, and Tuesday February 18th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2025, as noted by the symbol **DS1**

2.5 A 16nm 5.7TOPS CNN Processor Supporting Bi-Directional FPN for Small-Object Detection on High-Resolution Videos

2.6 1.78mJ/Frame 373fps 3D GS Processor Based on Shape-Aware Hybrid Architecture Using Earlier Computation Skipping and Gaussian Cache Scheduler

2.7 IRIS: An 8.55mJ/frame Spatial Computing SoC for Interactable Rendering and Surface-Aware Modeling with 3D Gaussian Splatting

2.9 STEP: An 8K-60fps Space-Time Resolution-Enhancement Neural-Network Processor for Next-Generation Display and Streaming

4.2 A 1.8-to-3.0GHz Fully Integrated All-In-One CMOS Frequency Management Module Achieving -47/+42ppm Inaccuracy from -40 to 95°C and -150/+70ppm After Accelerated Aging

4.3 A 0.36nW, 820μm², 32kHz Conduction-Angle-Adaptive Crystal Oscillator in 28nm CMOS for Real-Time Clock Applications

6.1 A 3-Stacked Hybrid-Shutter CMOS Image Sensor with Switchable 1.2μm-Pitch 50Mpixel Rolling Shutter and 2.4μm-Pitch 12.5Mpixel Global Shutter Modes for Mobile Applications

7.2 A 2.2pJ/b 212.5Gb/s PAM-4 Transceiver with >46dB Reach in 5nm FinFET

7.4 A 112Gb/s DSP-Based PAM-4 Receiver with an LC-Resonator-Based CTLE for >52dB Loss Compensation in 4nm FinFET

7.6 A 2.06pJ/b 106.25Gb/s PAM-4 Receiver with 3-Tap FFE and 1-Tap Speculative DFE in 28nm CMOS

8.8 Fine-Grained Spatial and Temporal Thermal Profiling of a 16nm CMOS Buck Converter and SOC Load-Current Emulator Using Low-Voltage Micron-Scale Thermal Sensors

8.9 An On-Cell Monitoring and Balancing System with Near-Field Communications for EV Batteries

9.6 A 6.78MHz Single-Stage Regulating Rectifier with Dual Outputs Simultaneously Charged in a Half Cycle Achieving 92.2% Efficiency and 131mW Output Power

10.1 A 77GHz Hybrid TDMA-MIMO Phased-Array Radar with 186m Detection Range and 3cm Range Resolution

10.5 A 28nm Multimode Multiband RF Transceiver with Harmonic-Rejection TX and Spur-Avoidance RX Supporting LTE Cat1bis

13.2 An 8.62μW 75dB-DR_{SoC} End-to-End Spoken-Language-Understanding SoC with Channel-Level AGC and Temporal-Sparsity-Aware Streaming-Mode RNN

13.3 A Cryo-BiCMOS Controller for $^{9}Be^{+}$-Trapped-Ion-Based Quantum Computers

13.4 Xiling: Cryo-CMOS 18-bit Dual-DAC Manipulator with 4.6μV Precision and 4.1nV/$Hz^{0.5}$ Noise Co-Integrated with the Single Electron Transistor at 60mK

14.3 A 28nm 17.83-to-62.84TFLOPS/W Broadcast-Alignment Floating-Point CIM Macro with Non-Two's-Complement MAC for CNNs and Transformers

16.1 Tomahawk5: 51.2Tb/s 5nm Monolithic Switch Chip for AI/ML Networking

16.2 RNGD: A 5nm Tensor-Contraction Processor for Power-Efficient Inference on Large Language Models

Digital Techniques for System Adaptation, Power Management and Clocking

Session Chair: Heein Yoon, *Ulsan National Institute of Science and Technology, Ulsan, Korea*
Session Co-Chair: Ben Calhoun, *University of Virginia, Charlottesville, VA*

8:00 AM

8.1 Dynamic Guard-Band Features of the IBM zNext System

T. Webel[1], P. J. Restle[2], R. Bertran[2], A. Buyuktosunoglu[2], S. M. Carey[3], A. Cook[1], K. Anderson[3], M. Romain[3], T. Strach[1], P. Bhadravati Parashurama[4], A. Tadkase[4], R. A. Tahir[1], L. Jenkins[3], K. Low[3], E. Engler[1]

[1]IBM Systems, Böblingen, Germany
[2]IBM Research, Yorktown Heights, NY
[3]IBM Systems, Poughkeepsie, NY
[4]IBM Systems, Bangalore, India

8:25 AM

8.2 Run-Time Power Management System by On-Die Power Sensor with Silicon Machine Learning-Based Calibration in a 3nm Octa-Core CPU

C-Y. Lu[1], B-J. Huang[1], M-C. Chen[1], A. Tsai[1], E-W. Fang[1], Y. Cho[1], R-Y. Liu[1], E. Wang[1], Y-M. Tsao[1], H. Mair[2], S-A. Hwang[1]

[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Austin, TX

8:50 AM

8.3 A Dynamically Reconfigurable Digital-Integrated Voltage-Regulator Fabric for Energy-Efficient DVFS in Multi-Domain SoCs

J. Arenas, C-H. Huang, K. Patino-Sosa, J-J. Park, H. S. Ozturk, V. Sathe
Georgia Institute of Technology, Atlanta, GA

9:15 AM

8.4 A 4GHz, 0.69%-Accuracy Voltage-Droop Detector with Multiple Remote Sensing and Under 2-Cycle Detection Latency in 2nm GAAFET

D. Jung, D. Lee*, S. Kim, S. Kim, M. Y. Kang, T. Nomiyama, D. Kim, J. Lee*
Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

Break 9:40 AM

10:05 AM

8.5 A Command-Aware Hybrid LDO for Advanced HBM Interfaces with 150µA Quiescent Current and 20pF On-Chip Capacitor Achieving Sub-10mV Voltage Droop in 400ps Settling Time

J. Kim[1], M. Han*[1], J. Bang[1,2], Y. Lim[3], J. Choi[1]*

[1]Seoul National University, Seoul, Korea
[2]KAIST, Daejeon, Korea
[3]Kyung Hee University, Yongin, Korea
*Equally Credited Authors (ECAs)

10:30 AM

8.6 A 0.024mm² All-Digital Fractional Output Divider with 257fs Worst-Case Jitter Using Split-DTC-Based Background Calibration

Y. Yu[1,2], D. Luo[1], J. Chen[1], Y. Guo[1], B. Liang[1], Y. Chi[1], H. Sun[1], J. Xiao[2], H. Gao[3], M. Tao[2], K. Tang[2]

[1]National University of Defense Technology, Changsha, China
[2]Hunan University, Changsha, China
[3]Southeast University, Nanjing, China

10:55 AM

8.7 A Dual V_{DD}-Temperature Sensor Employing Sensor Fusion with 2.4°C, 9mV (±3σ) Inaccuracy in 65nm CMOS

H. S. Ozturk[1], J. Arenas[1], C. Tokunaga[2], N. Kurd[2], V. Sathe[1]

[1]Georgia Institute of Technology, Atlanta, GA
[2]Intel, Hillsboro, OR

11:20 AM

8.8 DS1 Fine-Grained Spatial and Temporal Thermal Profiling of a 16nm CMOS Buck Converter and SOC Load-Current Emulator Using Low-Voltage Micron-Scale Thermal Sensors

Z. Ahmed, S. Kim, C. Augustine, H. K. Krishnamurthy, K. Ravichandran, J. W. Tschanz, V. De

Intel, Hillsboro, OR

11:35 AM

8.9 DS1 An On-Cell Monitoring and Balancing System with Near-Field Communications for EV Batteries

D. McMitchell, S. Foster, S. Block, M. Manson, S. Quinn, J. Sylvester

Dukosi, Edinburgh, United Kingdom

Conclusion 11:50 AM

Ubiquitous Power Delivery

Session Chair: Dongsu Kim, *Samsung Electronics, Gyeonggi, Korea*
Session Co-Chair: *Chen-Yen Ho, MediaTek, Hsinchu, Taiwan*

8:00 AM

9.1 An 85-to-230V_{AC} to 3.3-to-4.6V_{DC} 1.52W Capacitor-Drop Sigma-Floating-SC AC-DC Converter with 81.3% Peak Efficiency

F. Song[1], S. Han*[1,2], R. P. Martins[1], Y. Lu[1,2]*

[1]University of Macau, Macau, China
[2]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

8:25 AM

9.2 A 400MHz Symbol-Power-Tracking (SPT) Supply Modulator with SPT-Adaptive-Biasing Network Supporting 5G FR2 CMOS PA

J. Baek, A. Niknejad

University of California, Berkeley, CA

8:50 AM

9.3 A 74W/48V Monolithic-GaN Integrated Adjustable Multilevel Supply Modulator for 5G Base-Station Massive-MIMO Arrays

H. M. Pham[1], P. Asbeck[1], D. F. Kimball[1], N. Sharma[2], S. Dong[2], M. Shahshahani[2], W. S. Choi[2], G. Xu[2], M. Michel[3], R. Das[3,4], R. Beach[3], H-P. Le[1]

[1]University of California, San Diego, CA
[2]Samsung Research America, Plano, TX
[3]Efficient Power Conversion, El Segundo, CA
[4]University of Minnesota-Twin Cities, Minneapolis, MN

9:15 AM

9.4 A 102ns/V 94.3%-Peak-Efficiency Symbol-Power-Tracking Supply Modulator for 5G NR Power Amplifiers

M. Shang, B. Wang, C. Chen, J. Jin, L. Cheng

University of Science and Technology of China, Hefei, China

9:30 AM

9.5 A Sub-1V, 50mV Dropout LDO Using Pseudo-Impedance Buffer with Phase-Margin Improvement Design

Y-J. Jeon, J-H. Kim, W-G. Kim, S-W. Hong

Sogang University, Seoul, Korea

Break 9:45 AM

10:05 AM

9.6 DS1 A 6.78MHz Single-Stage Regulating Rectifier with Dual Outputs Simultaneously Charged in a Half Cycle Achieving 92.2% Efficiency and 131mW Output Power

Q. Zhuang[1], J. Sun[1], B. Li[1], J. Lu[1], X. Zhang[2], Y. Shi[1], H. Qiu[1]

[1]Nanjing University, Nanjing, China
[2]IBM T. J. Watson Reseach Center, Yorktown Heights, NY

10:30 AM

9.7 A 6.78MHz 94.2% Peak Efficiency Class-E Transmitter with Adaptive Real-Part Impedance Matching and Imaginary-Part Phase Compensation Achieving a 33W Wireless-Power-Transfer System

Y. Xiong, W. Cao, X. Liu, S. Zhao, Z. Xue, Z. Guo, L. Geng

Xi'an JiaoTong University, Xi'an, China

10:55 AM

9.8 A 50W 98%-Efficiency High-Power Wireless-Charging System with an Acoustic Noise-Reduced ASK Modulation Technique and Internal Hybrid Voltage-/Current-Mode ASK Demodulation

S. Oh, H. Kim, H. Kim, G. Namgoong, W. Park, S. Heo, J. Kim, S. Moon, H-S. Oh, H. Yu

Samsung Electronics, Hwaseong, Korea

11:20 AM

9.9 A Bi-Directional Dual-Path Boost-48V-Buck Hybrid Converter for High-Voltage Power-Transmission Cable in Light-Weight Humanoid Robots

W. Yang[1,2], Z. Tong*[1], J. Huang[1], R. P. Martins[1], Y. Lu[1,2,3]*

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China
[3]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

11:35 AM

9.10 A 93%-Peak-Efficiency Battery-Input 12-to-36V-Output Inductor-in-the-Middle Hybrid Boost Converter with Continuous Input and Output Currents and Fast Transient with No RHP Zero

Y. Jiang[1,2], Y. Lu[2,3], T. Tang[1], J. Jiang[1]

[1]Southern University of Science and Technology, Shenzhen, China
[2]University of Macau, Macau, China
[3]Tsinghua University, Beijing, China

11:50 AM

9.11 A 98.3%-Peak-Efficiency Single-Mode Hybrid Buck-Boost Converter with 7mV Maximum Output Ripple for Li-Ion Battery Management

J. Jin[1], R. Yang[1], W. Xu[2], L. Cheng[1]

[1]University of Science and Technology of China, Hefei, China
[2]Hefei CLT Microelectronics, Hefei, China

Conclusion 12:05 PM

Transceiver Chipsets for Communication and Radar

Session Chair: Matteo Bassi, *Infineon Technologies AG, Villach, Austria*
Session Co-Chair: Shahriar Shahramian, *Nokia – Bell Labs, New Providence, NJ*

8:00 AM

10.1 DS1 A 77GHz Hybrid TDMA-MIMO Phased-Array Radar with 186m Detection Range and 3cm Range Resolution

Z. Zhang, Y. Lu*, W. Xu, B. Cui, C. Hu, Z. Zhang, S. Sun, Z. Ren, C. Zhang, Z. Wang, G. Chen, C. Shi, L. Huang, L. Xu, R. Zhang*

East China Normal University, Shanghai, China
*Equally Credited Authors (ECAs)

8:25 AM

10.2 A 132-to-148GHz CMOS 4TX-4RX FMCW Radar Transceiver Array with Cavity-Backed Antenna-in-Package Achieving 28dBm EIRP

B. Liu, J. Huang, Z. Yang, X. Li, J. Zhang, X. Wang, H. Shi, F. Li, Z. Xu, R. Liu, S. Li, Y. Wang, K. Wang, H. Fu, F. Meng, K. Ma

Tianjin University, Tianjin, China

8:50 AM

10.3 A D-Band 2D-Scalable 4×4 Active Reflective Relay with Orthogonally Polarized On-Chip TX/RX Antennas and In-Front-End Common-Centroid Fast Azimuth/Elevation Angle-of-Arrival Detection

B. A. Abdelmagid, B. Lin, H. Wang

ETH Zürich, Zürich, Switzerland

9:15 AM

10.4 A 2-TRX IR-UWB Transceiver with Shared Antennas Supporting Channels 5 to 12 in Compliance with IEEE 802.15.4/4z Standards

H-G. Seok, J. Lee, S. Kim, W. Jung, H. Han, J. Kim, S. Kang, C. Kim, W. Kim, J. Cho, S. Bae, Y. Lee, S. Kim, H. Son, J. Jang, T. Kim, S. Cho, M. Cho, C. Ahn, H. Sung, W. Kim, S. Oh, J. Lee, H. Ko, J. Kim

Samsung Electronics, Hwaseong, Korea

9:30 AM

10.5 DS1 A 28nm Multimode Multiband RF Transceiver with Harmonic-Rejection TX and Spur-Avoidance RX Supporting LTE Cat1bis

F. Song[1], Z. Liu[1,2], D. Li[3], J. Ye[1], H. Deng[1], Y. Tan[1], Z. Zhang[1], J. Tao[1], S. Sun[3], L. Wang[3], X. Wan[3], Y. Jiang[1], H. Zhu[1], J. Ru[1,2], J. Zhang[1], J. Xiao[1]

[1]XINYI Information Technology, Shanghai, China
[2]Peking University, Beijing, China
[3]XINYI Semi, Singapore, Singapore

Break 9:45 AM

RF and mm-Wave Wireless Receivers

Session Chair: Negar Reiskarimian, *Massachusetts Institute of Technology, Cambridge, MA*

Session Co-Chair: Hao Gao, *Southeast University, Nanjing, China*

10:05 AM

11.1 A 256-Element Ka-Band CMOS Phased-Array Receiver Using Switch-Type Quadrature-Hybrid-First Architecture for Small Satellite Constellations DS2

S. Kato[1], J. Mayeda[1], K. Yuasa[1], M. Ide[1], T. Ota[1], S. Date[1], Y. Yamazaki[1], X. Wang[1], X. Fu[1], D. You[1], M. Higaki[2], J. Sudo[2], H. Takizawa[2], M. Shirakura[2], T. Tomura[1], H. Sakai[1], K. Kunihiro[1], K. Okada[1], A. Shirane[1]

[1]Institute of Science Tokyo, Tokyo, Japan
[2]Axelspace, Tokyo, Japan

10:30 AM

11.2 A Blocker-Tolerant Receiver with VCO-Based Non-Uniform Multi-Level Time-Approximation Filter with -36dB EVM in 28nm CMOS

C. Yang[1,2], S. Su[1,3], M. Ayesh[1], S. Mahapatra[1], M. Hamada[1], V. Chenna[1], H. Hashemi[1], M. S-W. Chen[1]

[1]University of Southern California, Los Angeles, CA
[2]d-Matrix, Santa Clara, CA
[3]University of Waterloo, Waterloo, Canada

10:55 AM

11.3 A Compact Full-Duplex Receiver with Wideband Multi-Domain Hilbert-Transform-Equalization Cancellation Based on Multi-Stage APFs Achieving 65dB SIC Across 120MHz BW

X. Ma, W. Li , S. Dong , R. Lyu, F. Chen , Y. Pu , C. Wang , H. Xu

Fudan University, Shanghai, China

11:20 AM

11.4 A Gm-C RF Quadrature-Current-Generation Technique with 40dB IRR in 0.65V 2mW Multi-Mode CMOS GNSS Receiver DS2

C. Chen[1], W. Xiang[2], Y. Zhao[1], X. Su[2], J. Chen[2], J. Yang[1]

[1]Southeast University, Nanjing, China
[2]Nanjing Low Power IC Technology Institute, Nanjing, China

11:45 AM

11.5 A 200MHz-BW Blocker-Tolerant Receiver with Fifth-Order Filtering Achieving 19dBm Adjacent-Channel IIP3

L. Lei, Y. Chen, Y. Li, Z. Hong, Y. Huang

Fudan University, Shanghai, China

Conclusion 12:00 PM

Innovations from Outside the (ISSCC's) Box

Session Chair: Kaushik Sengupta, *Princeton University, Princeton, NJ*
Session Co-Chair: Firooz Aflatouni, *University of Pennsylvania , Philadelphia, PA*

8:00 AM

12.1 Circuits that Solve Optimization Problems by Exploiting Physics Inequalities

E. Yablonovitch, Q. Feng, S. Vadlamani, P. Xiao

University of California, Berkeley, CA

8:25 AM

12.2 p-Circuits: Neither Digital nor Analog

M-C. Li[1], A. Ghosh[1], R. Jaiswal[1], L. A. Ghantasala[1,2], B. Behin-Aein[2], S. Sen[1], S. Datta[1]

[1]Purdue University, West Lafayette, IN
[2]Ludwig Computing, Mill Valley, CA

8:50 AM

12.3 Reversing Scattering to Perform Deep-Tissue Optical Imaging and the Current Need for a Suitable Optoelectronic Solution

C. Yang

California Institute of Technology, Pasadena, CA

9:15 AM

12.4 Skin-Inspired Electronics: An Emerging Sensing and Computing Platform

M. Ronchini[1,2], W. Wang[1], Y. Nishio[1], Y. Yao[1], Z. Bao[1]

[1]Stanford University, Stanford, CA
[2]Aarhus University, Aarhus, Denmark

Break 9:40 AM

Cool Computation Circuits

Session Chair: Joseph Bardin, *Google & UMass Amherst, Santa Barbara, CA*
Session Co-Chair: Shawn Hsu, *National Tsing Hua University, Hsinchu, Taiwan*

10:05 AM

13.1 A 0.22mm² 161nW Noise-Robust Voice-Activity Detection Using Information-Aware Data Compression and Neuromorphic Spatial-Temporal Feature Extraction

*Y. Liu*1, J. Li*1, Q. Zhang*1, T. Zhao[2], C. Shi[1], N. Shang[1], P. Chen[2], X. Ge[3], Y. Ma[1], L. Shen[1], Z. Wang[3], R. Huang[1], L. Ye[1,2]*

[1]Peking University, Beijing, China
[2]Advanced Institute of Information Tecnhology of Peking University, Hangzhou, China
[3]Nano Core Chip Electronic Technology, Hangzhou, China
*Equally Credited Authors (ECAs)

10:30 AM

13.2 DS1 An 8.62µW 75dB-DR_{SoC} End-to-End Spoken-Language-Understanding SoC with Channel-Level AGC and Temporal-Sparsity-Aware Streaming-Mode RNN

S. Zhou[1], Z. Li[1], T. Delbruck[1], K. Kim[2], S-C. Liu[1]

[1]University of Zurich and ETH Zurich, Zurich, Switzerland
[2]Aalto University, Espoo, Finland

10:55 AM

13.3 DS1 A Cryo-BiCMOS Controller for $^{9}Be^{+}$-Trapped-Ion-Based Quantum Computers

P. Toth[1], P. E. Shine[1], S. Halama[2], Y. Kudabay[1], K. Yamashita[1,3], H. Ishikuro[3], C. Ospelkaus[2], V. Issakov[1]

[1]Technische Universität Braunschweig, Braunschweig, Germany
[2]Leibniz University Hannover, Hannover, Germany
[3]Keio University, Yokohama, Japan

11:20 AM

13.4 DS1 Xiling: Cryo-CMOS 18-bit Dual-DAC Manipulator with 4.6µV Precision and 4.1nV/$Hz^{0.5}$ Noise Co-Integrated with the Single Electron Transistor at 60mK

Y. Li[1], Y. Zhang[2], H. Lin[3], C. Wang[1]

[1]University of Electronic Science and Technology of China, Chengdu, China
[2]Southern University of Science and Technology, Shenzhen, China
[3]Chengdu Data Automation System Technologies, Chengdu, China

11:35 AM

13.5 An 18.5µW/qubit Cryo-CMOS Charge-Readout IC Demonstrating QAM Multiplexing for Spin Qubits

Q. Schmidt[1], B. Jadot[1], B. Martinez[1], A. Faurie[1], T. Meunier[2], J-B. Casanova[3], X. Jehl[4], Y. Thonnart[3], F. Badets[1]

[1]CEA-Léti, Grenoble, France; [2]Quobly, Grenoble, France
[3]CEA-List, Grenoble, France; [4]CEA-Pheliqs, Grenoble, France

11:50 AM

13.6 A Via-Programmable DNN-Processor Fabrication Toward 1/40th Mask Cost

J. Shin, R. Sumikawa, D. Li, M. Hamada, A. Kosuge

University of Tokyo, Tokyo, Japan

Conclusion 12:05 PM

Compute-In-Memory

Session Chair: Saekyu Lee, *EnCharge AI, Denver, CO*
Session Co-Chair: Xueqing Li, *Tsinghua University, Beijing, China*

8:00 AM

14.1 A 22nm 104.5TOPS/W μ-NMC-Δ-IMC Heterogeneous STT-MRAM CIM Macro for Noise-Tolerant Bayesian Neural Networks

D-Q. You[1], W-S. Khwa*[2], B. Zhang[3], F-Y. Chen[1], A. Lee[1], Y-C. Hung[1], Y-M. Li[1], Y-H. Wang[1], C-C. Lo[1], R-S. Liu[1], K-T. Tang[1], C-C. Hsieh[1], Y-D. Chih[4], T-Y. J. Chang[4], M-F. Chang[1,2]*

[1]National Tsing Hua University, Hsinchu, Taiwan
[2]TSMC Corporate Research, Hsinchu, Taiwan
[3]TSMC Corporate Research, San Jose, CA
[4]TSMC, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

8:25 AM

14.2 A 16nm 216kb, 188.4TOPS/W and 133.5TFLOPS/W Microscaling Multi-Mode Gain-Cell CIM Macro for Edge-AI Devices

W-S. Khwa[1], P-C. Wu*[2], J-W. Su[2,3], C-Y. Cheng[2], J-M. Hsu[2], Y-C. Chen[2], L-J. Hsieh[2], J-C. Bai[2], Y-S. Kao[2], T-H. Lou[2], A. S. Lele[4], J-J. Wu[1], J-C. Tien[2], C-C. Lo[2], R-S. Liu[2], C-C. Hsieh[2], K-T. Tang[2], M-F. Chang[1,2]*

[1]TSMC Corporate Research, Hsinchu, Taiwan
[2]National Tsing Hua University, Hsinchu, Taiwan
[3]Industrial Technology Research Institute, Hsinchu, Taiwan
[4]TSMC Corporate Research, San Jose, CA
*Equally Credited Authors (ECAs)

8:50 AM

14.3 DS1 A 28nm 17.83-to-62.84TFLOPS/W Broadcast-Alignment Floating-Point CIM Macro with Non-Two's-Complement MAC for CNNs and Transformers

X. Wang[1,2], T. Jiao*[1], Y. Yang[1], S. Li[1], D. Li[1], A. Guo[1], Y. Shi[1], Y. Tang[1], J. Chen[1], Z. Zhang[1], Z. Liu[1], B. Liu[1], W. Shan[1], X. Wang[3], H. Cai[1], W. Zhu[3], J. Yang[1,2], X. Si[1]*

[1]Southeast University, Nanjing, China
[2]National Center of Technology Innovation for EDA, Nanjing, China
[3]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

9:15 AM

14.4 A 51.6TFLOPS/W Full-Datapath CIM Macro Approaching Sparsity Bound and <2^{-30} Loss for Compound AI

Z. Yue, X. Xiang*, Y. Wang, R. Guo, H. Han, S. Wei, Y. Hu, S. Yin*
Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

Break 9:40 AM

10:05 AM

14.5 A 28nm 192.3TFLOPS/W Accurate/Approximate Dual-Mode-Transpose Digital 6T-SRAM CIM Macro for Floating-Point Edge Training and Inference

Y. Yuan[1,2], B. Zhang[1,2], Y. Yang[3], Y. Luo[1,2], Q. Chen[3], S. Lv[3], H. Wu[1,2], C. Ma[1,2], M. Li[1,2], J. Yue[1], X. Wang[3], G. Xing[1], P-I. Mak[4], X. Li[3], F. Zhang[1]

[1]Institute of Microelectronics of the Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China
[3]Beijing Institute of Technology, Beijing, China
[4]University of Macau, Macau, China

10:30 AM

14.6 A 28nm 64kb Bit-Rotated Hybrid-CIM Macro with an Embedded Sign-Bit-Processing Array and a Multi-Bit-Fusion Dual-Granularity Cooperative Quantizer

X. Chen, S. Li, Z. Zhang, W. Zheng, X. Tan, Y. Tang, Y. Shi, L. Ren, Y. Mai, F. Liu, J. Chen, Z. Zhang, A. Guo, T. Xiong, B. Wang, X. Liu, W. Shan, B. Liu, H. Cai, J. Yang, X. Si

Southeast University, Nanjing, China

10:55 AM

14.7 NeuroPilot: A 28nm, 69.4fJ/node and 0.22ns/node, 32×32 Mimetic-Path-Searching CIM-Macro with Dynamic-Logic Pilot PE and Dual-Direction Searching

A. Guo[1], J. Zhang*[1], X. Pu[1], Y. Yang[1], D. Wu[1], Y. Tang[1], Y. Shi[1], Y. Gao[1], Z. Liu[1], B. Wang[1], T. Xiong[1], Z. Zhang[1], X. Chen[1], J. Chen[1], F. Liu[1], X. Wang[1], X. Liu[1], W. Shan[1], B. Liu[1], H. Cai[1], X. Si[1], J. Yang[1,2]*

[1]Southeast University, Nanjing, China
[2]National Center of Technology Innovation for EDA, Nanjing, China
*Equally Credited Authors (ECAs)

Conclusion 11:20 AM

Neural Interfaces and Edge Intelligence for Medical Devices

Session Chair: Azita Emami, *California Institute of Technology, Pasadena, CA*
Session Co-Chair: Taekwang Jang, *ETH Zurich , Zurich, Switzerland*

8:00 AM

15.1 A 3.9mW 200words/min Neural Signal Processor in Speech Decoding for Brain-Machine Interface

T-Y. Chang, J-B. Wang, Y-H. Tsai, C-H. Yang
National Taiwan University, Taipei, Taiwan

8:25 AM

15.2 A 1024-Channel 0.00029mm²/ch 74nW/ch Online Spatial Spike-Sorting Chip with Event-Driven Spike Detection and Self-Organizing Map Clustering

A. Akhoundi[1], Y. Landbrug[1], P. Yan[2], E. J. Chichilnisky[2], B. Murmann[3], D. G. Muratore[1]
[1]Delft University of Technology, Delft, The Netherlands
[2]Stanford University, Stanford, CA
[3]University of Hawaii, Honolulu, HI

8:50 AM

15.3 A 65nm Uncertainty-Quantifiable Ventricular Arrhythmia Detection Engine with 1.75μJ per Inference DS2

J. Liu, Z. Enciso, B. Cheng, L. Pei, S. Davis, Y. Qin, Z. Jia, X. S. Hu, Y. Shi, N. Cao
University of Notre Dame, Notre Dame, IN

9:15 AM

15.4 A Neuroprosthetic SoC with Sensory Feedback Featuring Frequency-Splitting-Based Wireless Power Transfer with 200Mb/s 0.67pJ/b Backscatter Data Uplink and Unsupervised Multi-Class Spike Sorting

Y. Huang[1], B. Liu[1], Y. Hou[1], J. Xu[1], H. You[1], A. Hung[1], S. Ghosh[1], E. Liu[1], N. Yang[1], J. Ma[1], H. Cai[1], L. Kondrataviciute[1,2], Q. Deng[1], S. K. Kalia[1,2], A. G. Richardson[3], P-H. Hsieh[4], R. Genov[1], X. Liu[1]
[1]University of Toronto, Toronto, Canada
[2]Toronto Western Hospital, Toronto, Canada
[3]University of Pennsylvania, Philadelphia, PA
[4]National Tsing Hua University, Hsinchu, Taiwan

Break 9:40 AM

10:05 AM

15.5 Event-Based Spatially Zooming Neural Interface IC with 10nW/Input Reconfigurable-Inverter Fabric and Input-Adaptive Quantization

J. Xu[1], M. Kanchwala[1], M. Abdolrazzaghi[1], H. Cai[1], Y. Huang[1], J. Ma[1], C. Lim[1], L. Xu[1], S. Gong[1], W. Deng[1], Q. Deng[1], J. Che[1], S. Nag[1], J. Olorocisimo[1], R. Singh[1], Y. Wang[1], J. S. Filho[1], M. Mohaved[2], H. Moradi[2], G. Eleftheriades[1], T. Valiante[2,3], R. Genov[1]

[1]University of Toronto, Toronto, Canada

[2]Krembil Neuroscience Center, Toronto, Canada

[3]Toronto Western Hospital, Toronto, Canada

10:30 AM

15.6 A 3.47 NEF 175.2dB FOM_S Direct Digitization Front-End Featuring Delta Amplification for Enhanced Dynamic Range and Energy Efficiency in Bio-Signal Acquisition

K. Jeong[1], C. Livanelioglu[1], J. Liao[1], I. Lee[2], T. Jang[1]

[1]ETH Zürich, Zürich, Switzerland

[2]University of Pittsburgh, Pittsburgh, PA

10:55 AM

15.7 A 4.6μW 3.3-NEF Biopotential Amplifier with 133V_{PP} Common-Mode Interference Tolerance and 102dB Total Common-Mode Rejection Ratio for Two-Electrode Recording System

Y. Park[1], Y-J. Mo[2], J-H. Kim[3], G. Cauwenberghs[3], S-J. Kim[2]

[1]Ulsan National Institute of Science and Technology, Ulsan, Korea

[2]Sogang University, Seoul, Korea

[3]University of California, San Diego, CA

Conclusion 11:20 AM

Invited Industry

Session Chair: Alicia Klinefelter, *NVIDIA, Durham, NC*
Session Co-Chair: Vivek De, *Intel, Hillsboro, OR*

1:30 PM

16.1 Tomahawk5: 51.2Tb/s 5nm Monolithic Switch Chip for AI/ML Networking

DS1 DS2

A. Khamisy[1], M. Kalkunte[1], P. Del Vecchio[1], Y. Cheok[1], G. Barsky[1], K. Muth[1], R. Sharifi[2]

[1]Broadcom, San Jose, CA
[2]Broadcom, Irvine, CA

1:55 PM

16.2 RNGD: A 5nm Tensor-Contraction Processor for Power-Efficient Inference on Large Language Models

DS1 DS2

S. M. Lee[1], H. Kim[1], J. Yeon[1], M. Kim[1], C. Park[1], B. Bae[1], Y. Cha[1], W. Choe[1], J. Choi[1], Y. Choi[1], K. J. Han[2], S. Hwang[1], K. Jang[1], J. Jeon[1], H. Jeong[1], Y. Jung[1], H. Kim[1], S. Kim[1], S. Kim[1], W. Kim[1], Y. Kim[1], Y. Kim[1], H. Kwon[1], J. K. Lee[1], J. Lee[1], K. Lee[1], S. Lee[1], M. Noh[1], J. Park[1], J. Seo[1], J. Paik[1]

[1]FuriosaAI, Seoul, Korea
[2]Dongguk University, Seoul, Korea

2:20 PM

16.3 An On-Device Generative AI Focused Neural Processing Unit in 4nm Flagship Mobile SoC with Fan-Out Wafer-Level Package

J-S. Park, T. Lee, H. Lee, C. Park, Y. Cho, M. Kang, H. Lee, J. Kang, T. Jeon, D. Lee, Y. Kang, K. Kum, G. Lee, H. Lee, M. Kim, S. Kwon, S-B. Park, D. Kim, C. Jo, H. Chung, I. Kim , J. Lee

Samsung Electronics, Hwaseong, Korea

2:45 PM

16.4 SambaNova SN40L: A 5nm 2.5D Dataflow Accelerator With Three Memory Tiers for Trillion Parameter AI

R. Prabhakar, J. Zhou, D. Gandhi, Y. Choi, M. Khayatzadeh, K. Kim, U. Durairajan, J. Park, S. Sarkar, J. L. Shin

SambaNova Systems, Palo Alto, CA

Break 3:10 PM

Hardware Security

Session Chair: Takeshi Sugawara, *The University of Electro-Communications, Tokyo, Japan*
Session Co-Chair: Leibo Liu, *Tsinghua University, Beijing, China*

3:35 PM

17.1 Sensor-Less Laser Voltage-Probing Attack Detection via Run-Time-Leakage-Shift Monitoring with 4.35% Area Overhead

H. Zhang[1], L. Lin*[2], D. Xiong[1], M. B. Alioto[1]*

[1]National University of Singapore, Singapore, Singapore
[2]Southern University of Science and Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

4:00 PM

17.2 A 28nm 4.05μJ/Encryption 8.72kHMul/s Reconfigurable Multi-Scheme Fully Homomorphic Encryption Processor for Encrypted Client-Server Computing

S. Lu[1,2], W. Zhu[1,2], B. Yang[1,2], J. Yang[1,2], T. Dai[1,2], C. Chen[1,2], X. Han[1,2], J. Yang[3], H. Wang[1,2], M. Zhu[4], S. Wei[1,2], A. Zhang[1], L. Liu[1,2]

[1]Tsinghua University, Beijing, China
[2]Beijing National Research Center for Information Science and Technology (BNRist), Beijing, China
[3]Wuxi Research Institute of Applied Technologies, Tsinghua University, Beijing, China
[4]Micro Innovation Integrated Circuit Design, Wuxi, China

4:25 PM

17.3 A 30.4GOPS/mW MK-CKKS Processor for Secure Multi-Party Computation

L-H. Lin, Y-K. Yang, C-H. Yang

National Taiwan University, Taipei, Taiwan

4:50 PM

17.4 An Efficient V_{th}-Tilting PUF Design in 3nm GAA and 8nm FinFET Technologies

B. Karpinskyy, Y. K. Lee, S. Noh, Y. Choi, J. Park, J. Kang, T. Park, E. Oh, G. Kim, S. Lee, H. Ko, J. Shin, H-G. Rhew, J. Shin

Samsung Electronics, Hwaseong, Korea

5:05 PM

17.5 An Eye-Opening Arbiter PUF for Fingerprint Generation Using Auto-Error Detection for PVT-Robust Masking and Bit Stabilization Achieving a BER of 2e-8 in 28nm CMOS

B. Driemeyer, H. Mandry, D-P. Wiens, J. Becker, J. G. Kauffman, M. Ortmanns

University of Ulm, Ulm, Germany

5:20 PM

17.6 A 100MHz Self-Calibrating RC Oscillator Capable of Clock-Glitch Detection for Hardware Security in a 3nm FinFET Process

N. Mehta[1], S. Tell[2], S. Song[1], S. Kudva[1], B. Zimmer[1], M. Sinangil[1], C. T. Gray[2]

[1]Nvidia, Santa Clara, CA
[2]Nvidia, Durham, NC

Conclusion 5:35 PM

Noise-Shaping and SAR-Based ADCs

Session Chair: Xiyuan Tang, *Peking University, Beijing, China*
Session Co-Chair: Pieter Harpe, *Eindhoven University of Technology, Eindhoven, The Netherlands*

Session Chair: Ying-Zu Lin*, *Mediatek, Hsinchu, Taiwan*

1:30 PM

18.1 A Fully Dynamic Noise-Shaping SAR ADC Achieving 120dB SNDR and 189dB FoM_S in 1kHz BW

H. Zhao, X. Zhang*, Q. Deng, J. Hu, Z. Li, S. Yang, J. Liu*
University of Electronic Science and Technology of China, Chengdu, China
*Equally Credited Authors (ECAs)

1:55 PM

18.2 A 12.2µW 99.6dB-SNDR 184.8dB-FoM_S DT Zoom PPD ΔΣM with Gain-Embedded Bootstrapped Sampler

Y. Luan, X. Xu, J. Gao, J. Cui, Z. Chen, S. Ye, R. Huang, L. Shen
Peking University, Beijing, China

2:20 PM

18.3 A 93.3dB SNDR, 180.4dB FoM_S Calibration-Free Noise-Shaping Pipelined-SAR ADC with Cross-Stage Gain-Mismatch-Error-Shaping Technique and Negative-R-Assisted Residue Integrator

J. Gao, Y. Luan, S. Ye, X. Xu, Z. Chen, J. Cui, R. Huang, L. Shen
Peking University, Beijing, China

2:45 PM

18.4 A 184.8dB FoM_S 1.6MS/s Incremental Noise-Shaping Pipeline ADC with Single-Amplification-Based kT/C-Noise-Cancellation Technique

Z. Wang, B. Li, J. Tang, Z. Wu, H. Luo, Y. Wang, X. Tang
Peking University, Beijing, China

Break 3:10 PM

**1981 to 2024*

3:35 PM

18.5 A Rail-to-Rail 3rd-Order Noise-Shaping SAR ADC Achieving 105.4dB SFDR with Integrated Input Buffer Using Continuous-Time Correlated Level Shifting

S. Ye, J. Cui, J. Gao, J. Li, X. Zhang, R. Huang, L. Shen
Peking University, Beijing, China

4:00 PM

18.6 An Easy-Drive 16MS/s Pipelined-SAR ADC Using Split Coarse-Fine Input-Buffer-Sampling Scheme and Fast Robust Background Inter-Stage Gain Calibration

Z. Chen, S. Ye, J. Gao, J. Li, J. Cui, X. Xu, Y. Luan, R. Huang, L. Shen
Peking University, Beijing, China

4:25 PM

18.7 A 70dB SNDR 80MHz BW Filter-Embedded Pipeline-SAR ADC Achieving 172dB FoM$_S$ with Progressive Conversion and Floating-Charge-Transfer Amplifier

S. Huang, Z. Zhang, X. He, M. Gu, Y. Tao, Y. Zhong, N. Sun, L. Jie
Tsinghua University, Beijing, China

4:50 PM

18.8 A Cryo-CMOS 800MS/s 7b CI-SAR with only 4fF Input Capacitance and 64dB SFDR

B. Veraverbeke, F. Tavernier
KU Leuven ESAT-MICAS, Leuven, Belgium

Conclusion 5:15 PM

Frequency Synthesizers and Series-Resonance VCOs

Session Chair: Dmytro Cherniak, *Infineon Technologies, Villach, Austria*
Session Co-Chair: Wei Deng, *Tsinghua University, Beijing, China*

1:30 PM

19.1 A PVT-Robust 5.5GHz Fractional-N Cascaded RO-Based Digital PLL with Voltage-Domain Feedforward Noise Cancellation

Y. Duan[1], Y. Zhu[1], R. P. Martins[1,2], C-H. Chan[1]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

1:55 PM

19.2 A 96fs_{rms}-Jitter, -70.6dBc-Fractional-Spur Cascaded PLL Employing Two MMDs with Shared DSM for Quantization Noise Cancellation

H. Zhang, Y. Zhu*, M. Osada, T. Iizuka*

University of Tokyo, Tokyo, Japan
*Equally Credited Authors (ECAs)

2:20 PM

19.3 A Fractional-N PLL with 34fs_{rms} Jitter and -255.5dB FoM Based on a Multipath Feedback Technique

C-C. Hung, C-H. Shen, C-L. Lin, M. Tzou, K. Fong, Y-L. Hsueh

MediaTek, Hsinchu, Taiwan

2:45 PM

19.4 An 8.1-to-9.9GHz Single-Core Pseudo-Series-Resonance Oscillator Achieving -128.7dBc/Hz PN at 1MHz

J. Chen[1], K. Xu[2], T. Siriburanon[1], R. B. Staszewski[1]

[1]University College Dublin, Dublin, Ireland
[2]King's College London, London, United Kingdom

3:00 PM

19.5 A Differential Series-Resonance CMOS VCO with Pole-Convergence Technique Achieving 202.1dBc/Hz FoM_{TA} at 10MHz Offset

J. Guo, P. Qin, H. Zhu, X. Yi, W. Feng, W. Che, Q. Xue

South China University of Technology, Guangzhou, China

Break 3:15 PM

3:35 PM

19.6 A 60GHz I/Q-Calibrated SSB-Mixer-Based LO with Sub-ns Settling Time and -56dBc Worst-Case Spur Using ILO Filter in 28nm CMOS

J. Oh[1], C. So[2], H. Kim[3], S. Hong[1], S. Cho[1]

[1]KAIST, Daejeon, Korea
[2]University of California, Santa Babara, CA
[3]Korea Aerospace Research Institute, Daejeon, Korea

4:00 PM

19.7 A 27GHz Fractional-N Sub-Sampling PLL Achieving 57.9fs$_{rms}$ Jitter, -249.7dB FoM, and 1.98µs Locking Time Using a Polarity-Reversible SSPD

H. Li[1], J. Li[1], X. Jiang[1], X. Meng[1], J. Yin[1], R. P. Martins[1,2], P-I. Mak[1]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:25 PM

19.8 A 0.65V-V$_{DD}$ 10.4-to-11.8GHz Fractional-N Sampling PLL Achieving 73.8fs$_{rms}$ Jitter, -271.5dB FoM$_N$, and -61dBc In-band Fractional Spur in 40nm CMOS

X. Shen[1,2], Z. Zhang[1,2], Y. Li[1,2], J. Chen[1,2], X. Kong[1], N. Qi[1,2], J. Liu[1,2], N. Wu[1,2], L. Liu[1,2]

[1]Institute of Semiconductors, Chinese Academy of Sciences, Beijing, China
[2]University of Chinese Academy of Sciences, Beijing, China

4:50 PM

19.9 An 11-to-16.4GHz, 3.4GHz/µs-Slope, 5.32GHz-Chirp-Bandwidth, 0.043%-RMS-Frequency-Error FMCW Digital PLL with Posterior-Segment DPD Featuring 5-Chirp-Cycle Convergence Time

A. Yan, W. Deng, H. Jia, Y. Yang, C. Tang, S. Sun, Z. Wang, B. Chi

Tsinghua University, Beijing, China

5:05 PM

19.10 A 4.6GHz 63.3fsrms PLL-XO Co-Design Using a Self-Aligned Pulse-Injection Driver Achieving -255.2dB FoMJ Including the XO Power and Noise

C. Livanelioglu, L. He*, J. Gong*, S. Arjmandpour, G. Atzeni, T. Jang*

ETH Zürich, Zürich, Switzerland
*Equally Credited Authors (ECAs)

5:20 PM

19.11 A 13GHz Charge-Pump PLL Achieving 15.8fs$_{rms}$ Integrated Jitter and -98.5dBc Reference Spur

D. Sun[1], F. Bu[1], Q. Ye[1], S. Li[1], Y. Gao[1], B. Wang[1], H. Xu[2], N. Yan[2], S. Liu[1], Z. Zhu[1]

[1]Xidian University, Xi'an, China
[2]Fudan University, Shanghai, China

Conclusion 5:35 PM

Sensors and Actuators for Health and Autonomy

Session Chair: Milin Zhang, *Tsinghua University, Beijing, China*
Session Co-Chair: Kyeongha Kwon, *KAIST, Daejeon, Korea*

1:30 PM

20.1 A 3.5×3.5mm² 1.47mW/ch 16-Channel MSS-CMOS Heterogeneous Multi-Modal-Gas-Sensor Chip Stack

K. Naruse[1], N. Kato[1], T. Matsumori[1], J. Shiomi[1], Y. Midoh[1], T. Hirose[1], G. Imamura[1,2], G. Yoshikawa[2,3], C. Sideris[4], N. Miura[1]

[1]Osaka University, Suita, Japan
[2]National Institute for Materials Science, Tsukuba, Japan
[3]University of Tsukuba, Tsukuba, Japan
[4]University of Southern California, Los Angels, CA

1:55 PM

20.2 A 67μW/channel, 0.13nW/synapse/b Nose-on-a-Chip for Noninvasive Diagnosis of Diseases with On-Chip Incremental Learning

D. Huo[1], Y-H. Lin*[2], P. K. Shihabudeen[2], J. Zhang[1], T. Li[1], C-R. Chou[2], Z. Wang[1], K-T. Tang[2], H. Chen[1]*

[1]Tsinghua University, Beijing, China
[2]National Tsing Hua University, Hsinchu, Taiwan
*Equally Credited Authors (ECAs)

2:20 PM

20.3 An RFID-Inspired One-Step Packaged Multimode Bio-Analyzer with Vacuum Microfluidics for Point-of-Care Diagnostics

Y-T. Hsiao[1], Y-C. Tsai[1], W. Foo[1], H-Y. Hou[1], Y-C. Su[2], Y. L. Li[1], J-C. Chien[1]

[1]University of California, Berkeley, CA
[2]National Taiwan University, Taipei City, Taiwan

2:45 PM

20.4 DS2 MEMS-Free 4096-Pixel CMOS E-Nose Gas-Sensor Array with Molecular-Selective Metal-Organic-Framework Sensing and In-Pixel Thermodynamic Modulation for Fast Sensor Regeneration

M. Saif, F. Jiang*, S-W. Lo, A. Wang, Z. Huang, J. Wang, H. Liu, C-J. Shih, T. Burger, H. Wang*

ETH Zürich, Zürich, Switzerland
*Equally Credited Authors (ECAs)

3:00 PM

20.5 Millimeter-Sized 0.1pM LoD Wireless 16-Channel Organic-Electrochemical-Transistor-Based Electrochemical Sensing SoC

Y. Ma[1], S. Liu*[1], Y. Song[1], C. Xie[1], Y. Zhang[2], C. Sun[2], X. Ma[2], L. Yin[1], M. Zhang[1]*

[1]Tsinghua University, Beijing, China
[2]Beijing Ningju Technology, Beijing, China
*Equally Credited Authors (ECAs)

Break 3:15 PM

3:35 PM

20.6 Fully Integrated Self-Propelling Microrobot in 180nm CMOS with Sub-GHz Parity-Time-Symmetry On-Chip Energy Harvesting and Traveling Wave Electroosmosis Actuation

R. Cai, M. D. K. Niazi, Y. Ai, J. Zhu, L. Wu, X. Lu
Shanghai Jiao Tong University, Shanghai, China

4:00 PM

20.7 DS2 A 384-Site Chip Platform for Biochemical Applications with Individual Site Precision Temperature Control

M. Coln[1], Q. Meng*[1], V. Bucur[2], R. Lakshmanan[2], A. Yadav[1], D. Lloyd[3], N. Ferri[4], M. Bignell[4], D. Di Nuzzo[4], P. Nadeau[1], M. Hayes[4], R. Trogan[1]*
[1]Analog Devices, Boston, MA; [2]Analog Devices, Limerick, Ireland
[3]Analog Devices, San Jose, CA; [4]Evonetix, Cambridge, United Kingdom
*Equally Credited Authors (ECAs)

4:25 PM

20.8 A 94.8nW Battery-Free Intelligent Silicon Platform Enabling Distributed, Adaptive, and Event-Driven Multimodal Sensing at the Edge

H. Zhang[1], W-H. Yu[1], Z. Zhao[1], Z. Yang[1], K-F. Un[1], J. Yin[1], R. P. Martins[1,2], P-I. Mak[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

4:50 PM

20.9 An Autonomous and Lightweight Microactuator Driving System Using Flying Solid-State Batteries

Z. Lin[1], J. Wouda*[2], S. Oukassi[2], G. Pillonnet[2], P. Mercier[1]*
[1]University of California, San Diego, CA; [2]CEA-Léti, Grenoble, France
*Equally Credited Authors (ECAs)

5:05 PM

20.10 DS2 A 200GHz 200-Pixel 2D Near-Field Imager for Biomedical Applications

A. Ameri, J-C. Chien, A. Niknejad
University of California, Berkeley, CA

5:20 PM

20.11 DS2 A Crystal-less BodyID with an Asynchronous Clockless Leakage-Powered Wake-Up Receiver and Over-the-Channel Clock Recovery

L. Ding, A. Ghosh, S. Sen
Purdue University, West Lafayette, IN

5:35 PM

20.12 DS2 A 3×3.3mm Configurable γ Photon Spectrometer for Precision Radioguided Cancer Resection

R. Lall[1], Y. Seo[1,2], A. Niknejad[1], M. Anwar[1,2]
[1]University of California, Berkeley, CA
[2]University of California, San Francisco, CA

Conclusion 5:50 PM

Compute and USB Power

Session Chair: John Pigott, *NXP, Phoenix, AZ*
Session Co-Chair: Rinkle Jain, *Nvidia, Santa Clara, CA*

1:30 PM

21.1 A 12A 89.3% Peak Efficiency and 26mV Undershoot 12-to-1V Two-Stage Converter with Regulated Resonant Switched-Capacitor Regulators

S. Ren, Y. Du, M. Zhao, Z. Tan, C. Li, Y. Ding, W. Li, W. Qu

Zhejiang University, Hangzhou, China

1:55 PM

21.2 A Dual-Input Bidirectional 3-Level Battery Charger with Coarse-Fine V_{CF} Balancing and Wide VCR for Foldable Mobile Applications

W. Hong, H. Ko, J. So, W. Heo, Y. Cho, J. Yoo, H-S. Son, Y. Chung, D-J. Kim, Y. Park, B. Jin, S. Cho, M. Kwon, K. Park, D. Cho, J. W. Heo, S. Lee, S. Moon, H-S. Oh, H. Yu

Samsung Electronics, Hwaseong, Korea

2:20 PM

21.3 A Segmented-Interlacing Multi-Phase Hybrid Converter with Inherently Auto-Balanced I_Ls and Boosted I_L Slew Rate During Load Transients

J. Yang[1], R. P. Martins[1,2], M. Huang[1]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

2:45 PM

21.4 A 97.4%-Peak-Efficiency Always-Half-Inductor-Current Hybrid Bidirectional Converter with Adaptive Target Current Tracking for USB-to-2-Cell Bidirectional Power Transfer

Y. Lee, H. Park, M. Kim, W. Jung, H. Kim, H-M. Lee

Korea University, Seoul, Korea

3:00 PM

21.5 DS2 A Fully Integrated Multi-Phase Voltage Regulator with Enhanced Light-Load-Efficiency Peak of 86%, Featuring an Autonomous Mode Transition from Hard-Switching to Soft-Switching to Discontinuous Conduction Mode in 3nm FinFET CMOS

K. Joshi[1], A. Shreepathi Bhat[2], C. Schaef[2], K. Chen[3], E. Lee[2], Y. Kocharyan[1], A. Janardanan[2], D. Ganta[2], H. Zhang[3], M. Geppert[2], P. Mclaughlin[1], A. Raghavan[1], S. Masilamani[3], S. Askari[2], K. Livingston[2]

[1]Intel, Santa Clara, CA
[2]Intel, Hillsboro, OR
[3]Intel, Hudson, MA

Break 3:15 PM

3:35 PM

21.6 A 2A Fully Analog Distribution LDO with Noise Immunity for an SoC

J-H. Kim[1], Y-J. Jeon[1], W-G. Kim[1], J. Lee[2], J-H. Yang[2], S-W. Hong[1]

[1]Sogang University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea

4:00 PM

21.7 Merging Hybrid and Multi-Phase Topologies: A 6-Phase Triple-Step-Down DC-DC Converter Achieving up to a 60:1 Voltage Conversion Ratio and 868A/cm³ Current Density

M. H. K. Hmada[1], W-C. B. Liu[1], G. Pillonnet[2], P. Mercier[1]

[1]University of California, San Diego, CA
[2]CEA-Léti, Grenoble, France

4:25 PM

21.8 HOOP: A Scalable Hybrid DC-DC Converter Ring for High-Performance Computing

Z. Tong[*1], Z. Yu*[*1,2], J. Huang[1], X. Mao[1,3], B. Wicht[4], R. P. Martins[1], Y. Lu[1,2,3]*

[1]University of Macau, Macau, China
[2]Tsinghua University, Beijing, China
[3]UM Hetao IC Research Institute, Shenzhen, China
[4]Leibniz University Hannover, Hannover, Germany
*Equally Credited Authors (ECAs)

4:50 PM

21.9 A 20MHz & 1MHz Dual-Loop Non-Uniform-Multi-Inductor Hybrid DC-DC Converter with Specified Inductor Current Allocation and Fast Transient Response

J. Huang[*1], X. Mao*[*1,2], Z. Tong[1], Z. Yu[1], W. Yang[1], C-S. Lam[1], R. P. Martins[1], Y. Lu[1,2,3]*

[1]University of Macau, Macau, China
[2]UM Hetao IC Research Institute, Shenzhen, China
[3]Tsinghua University, Beijing, China
*Equally Credited Authors (ECAs)

Conclusion 5:15 PM

Memory Interface

Session Chair: Dongkyun Kim, *SK hynix, Icheon, Korea*
Session Co-Chair: Hidehiro Shiga, *KIOXIA, Yokohama, Japan*

3:35 PM

22.1 A 0.275pJ/b 42Gb/s/pin Clock-Referenced PAM3 Transceiver Tolerant to Supply Noise, Reference Offset and Crosstalk for Chiplets and Short-Reach Memory Interfaces

K. Kim[1], J-H. Park[2], H-J. Park[1], J. Park[1], J. Kim[1], W-S. Choi[1]

[1]Seoul National University, Seoul, Korea
[2]University of California, Berkeley, CA

4:00 PM

22.2 An 850μW 2-to-5GHz Jitter-Filtering and Instant-Toggling Injection-Locked Quadrature-Clock Generator for Low-Power Clock Distribution in HBM Interfaces

J. Seo[*1], Y. Cho*[*1,2], Y. Shin[1,2], J. Choi[1]*

[1]Seoul National University, Seoul, Korea
[2]KAIST, Daejeon, Korea
*Equally Credited Authors (ECAs)

4:25 PM

22.3 A 42Gb/s Single-Ended Hybrid-DFE PAM-3 Receiver for GDDR7 Memory Interfaces

B. Kim[*1], H. Chi*[*1], H. Ko[1], S. Byeon[1], S. Lee[1], C. Pyo[1], S. Kim[1], B. Kang[1], E. Song[1], K. Na[1], J. Cha[1], H. Kim[1], S. Park[1], W-S. Choi[2], K. Kim[1], H-K. Jung[1], J. Cho[1], J. Kim[1]*

[1]SK hynix, Icheon, Korea
[2]Seoul National University, Seoul, Korea
*Equally Credited Authors (ECAs)

4:50 PM

22.4 A 32-to-50Gb/s/pin Single-Ended PAM-4 Transmitter with a ZQ-Based FFE and PAM-4 LSB DBI-DC Encoding

Y. Jo[*1], H. Kim*[*1], Y. Choi[2], J. Park[2], M. Kwak[2], J. Han[1]*

[1]Hanyang University, Seoul, Korea
[2]Samsung Electronics, Hwaseong, Korea
*Equally Credited Authors (ECAs)

5:05 PM

22.5 A 0.3pJ/b 32Gb/s/pin Single-Ended PAM-4 Receiver with a Delay-less Capacitive-Feedback Equalizer

J. So, Y. Kwon, S. Park, S. Kim, C. Sim, H. Shin, S-B. Lee, T. Kim, C. Kim

Korea University, Seoul, Korea

Conclusion 5:20 PM

This year, the Demonstration Session extending in selected regular papers, both Academic and Industrial, will take place on Monday February 17th, and Tuesday February 18th, from 5 pm until 7 pm in the Golden Gate Hall. These demonstrations will feature real-life applications made possible by new ICs presented at ISSCC 2025, as noted by the symbol DS2

11.1 A 256-Element Ka-Band CMOS Phased-Array Receiver Using Switch-Type Quadrature-Hybrid-First Architecture for Small Satellite Constellations

11.4 A Gm-C RF Quadrature-Current-Generation Technique with 40dB IRR in 0.65V 2mW Multi-Mode CMOS GNSS Receiver

15.3 A 65nm Uncertainty-Quantifiable Ventricular Arrhythmia Detection Engine with 1.75µJ per Inference

16.1 Tomahawk5: 51.2Tb/s 5nm Monolithic Switch Chip for AI/ML Networking

16.2 RNGD: A 5nm Tensor-Contraction Processor for Power-Efficient Inference on Large Language Models

20.4 MEMS-Free 4096-Pixel CMOS E-Nose Gas-Sensor Array with Molecular-Selective Metal-Organic-Framework Sensing and In-Pixel Thermodynamic Modulation for Fast Sensor Regeneration

20.7 A 384-Site Chip Platform for Biochemical Applications with Individual Site Precision Temperature Control

20.10 A 200GHz 200-Pixel 2D Near-Field Imager for Biomedical Applications

20.11 A Crystal-less BodyID with an Asynchronous Clockless Leakage-Powered Wake-Up Receiver and Over-the-Channel Clock Recovery

20.12 A 3×3.3mm Configurable γ Photon Spectrometer for Precision Radioguided Cancer Resection

21.5 A Fully Integrated Multi-Phase Voltage Regulator with Enhanced Light-Load-Efficiency Peak of 86%, Featuring an Autonomous Mode Transition from Hard-Switching to Soft-Switching to Discontinuous Conduction Mode in 3nm FinFET CMOS

23.2 A 28nm 0.22µJ/Token Memory-Compute-Intensity-Aware CNN-Transformer Accelerator with Hybrid-Attention-Based Layer-Fusion and Cascaded Pruning for Semantic Segmentation

23.3 EdgeDiff: 418.4mJ/Inference Multi-Modal Few-Step Diffusion Model Accelerator with Mixed-Precision and Reordered Group Quantization

23.7 BROCA: A 52.4-to-559.2mW Mobile Social Agent System-on-Chip with Adaptive Bit-Truncate Unit and Acoustic-Cluster Bit Grouping

23.9 Slim-Llama: A 4.69mW Large-Language-Model Processor with Binary/Ternary Weights for Billion-Parameter Llama Model

25.2 A 4GS/s Fully Analog 256×256 MP-Based Cross-Correlator with 1000TOPS/W Compute Efficiency and 1.3TOPS/mm² Compute Density in 22nm SOI CMOS

27.1 A 3-Axis MEMS Gyroscope with 2.8ms Wake-Up Time Enabled by a 1.5µW Always-On Drive Loop

27.5 A 4,100µm² Wire-Metal-Based Temperature Sensor with a Fractional-Discharge FLL and a Time-Domain Amplifier with ±0.2°C Inaccuracy (3σ) from –40 to 125°C and 45fJ·K² Resolution FoM in 28nm CMOS

29.4 A 38Mb/mm² 380/540mV Dual-Rail SRAM in 3nm-FinFET Technology

36.3 A 0.29pJ/b 5.27Tb/s/mm UCIe Advanced Package Link in 3nm FinFET with 2.5D CoWoS Packaging

37.2 A 2-Dimensional mm-Scale Network-on-Textiles (kNOTs) for Wearable Computing with Direct Die-to-Yarn Integration of 0.6×2.15mm² SoC and bySPI Chiplets

37.4 SHINSAI: A 586mm² Reusable Active TSV Interposer with Programmable Interconnect Fabric and 512Mb 3D Underdeck Memory

37.7 A 28nm 18.1µJ/Acquisition End-to-End GPS Acquisition Accelerator with Energy-Accuracy-Driven Mixed-Radix IFFT and ROM-Assisted Computing

EVENING EVENTS Tuesday, February 18th, 8:00 PM

EE2:
Quantum Computing: Whose Qubit is Better?

Organizers: **Huichu Liu,** *Meta, Sunnyvale, CA*
Sally Amin, *Apple, Cupertino, CA*

Co-Organizers: **Kamala Raghavan,** *Qualcomm, San Diego, CA*
Elpida Karapepera, *University of Washington, Seattle, WA*
Shubha Bommalingaiahnapallya, *Intel, Hillsboro, OR*
Najme Ebrahimi, *Northeastern University, Boston, MA*
Alice Wang, *UT Dallas, Dallas, TX*
Zeynep Toprak Deniz, *IBM Research, Yorktown Heights, NY*
Farhana Sheikh, *Altera, Portland, OR*

Moderator: **Maud Vinet,** *Quobly, Grenoble, France*

Quantum computing utilizes principles of quantum mechanics to solve intricate computational problems more efficiently than classical computers. Various qubit technologies are being developed for this purpose, such as superconducting qubits, trapped ions, and silicon-spin qubits. Each approach has its supporters and critics with prominent industry players investing heavily in one or more of these technologies. The race is on to determine which qubit technology will emerge as the dominant choice. Be prepared to participate in a discussion with our panel of experts as they weigh in on the advantages and challenges associated with each of the innovative approaches to determine whose qubit will rise to the top.

Panelists: **Hanhee Paik,** *IBM, Tokyo, Japan*
Shirin Montazeri, *Google, San Diego, CA*
Sophie Beyne, *IMEC, Leuven, Belgium*
Jeanette Roberts, *Intel, Hillsboro, OR*

EE3:
Future of Analog Design: Still Magical or Mostly Digital?

Organizer: **Sudipto Chakraborty,** *IBM, Yorktown Heights, NY*
Co-Organizers: **Patrik Arno,** *STMicroelectronics, Grenoble, France*
Drew Hall, *University of California San Diego, San Diego, CA*
Shiyu Su, *University of Waterloo, Waterloo, Canada*
Brian Ginsburg, *Texas Instruments, Dallas, TX*

Moderator: **Chris Rudell,** *University of Washington, Seattle, WA*

A gradual paradigm shift has occurred over the past four decades for implementing analog functions in IC design from classical analog circuits to digital-intensive circuits. The emergence of new digital architectures has further prompted explosive growth in digital circuits providing analog functionality, including digital radios, transmitters (TXs), receivers (RXs), phase-locked loops (PLLs), low-dropout voltage regulators (LDOs), and time-based analog-to-digital converters (ADCs). The success of these new digital approaches has been further driven by improvements in area, power, and design time in advanced technology nodes. Classical analog circuits, however, often provide superior performance as compared to their digital counterparts. In this panel, experts across industry and academia will explore this digital/analog divide and provide insights into this IC design trade-off, including in the context of emerging technology trends.

Panelists: **Andreia Cathelin,** *STMicroelectronics, Crolles, France*
Reza Rofougaran, *Movandi, Irvine, CA*
Bram Nauta, *University of Twente, Enschede, Netherlands*
Kenichi Okada, *Institute of Science Tokyo, Tokyo, Japan*
Elad Alon, *Blue Cheetah, Sunnyvale, CA*
Nagendra Krishnapura, *Indian Institute of Technology, Chennai, India*

EE4:
The Next Decade of AI – Barriers, Opportunities, & Directions

Organizer: **Visvesh S. Sathe,** *Georgia Institute of Technology, Atlanta, GA*

Co-Organizers: **John Wuu,** *AMD, Fort Collins, CO*
Chih-Ming Hung, *MediaTek, Taipei, Taiwan*
Huichu Liu, *Meta, Sunnyvale, CA*

Moderator: **Naveen Verma**, *Princeton University, Princeton, NJ*

The past decade has witnessed dramatic advances in Artificial Intelligence (AI) hardware, software, and models, paving the way for AI applications that are shaping many facets of our everyday life. As AI ushers us into the next boom in autonomy, productivity, and creativity, there are critical challenges that lie ahead such as energy consumption, costs, data availability, and government regulations to name a few. Which of these or other potential barriers will limit AI progress in the next decade? What will be the unintended consequences of the emergence of AI and what can we do to curb these? Which opportunities may arise from innovating solutions to overcome these challenges? Our evening panel of experts in AI hardware, software, models, and government policy offer insightful perspectives on these and other consequential questions that will influence the course of AI in the coming decade.

Panelists: **Richard Ho,** *OpenAI, Palo Alto, CA*
Nikhil Jayaram, *Google, San Francisco, CA*
Carole-Jean Wu, *Meta, Cambridge, MA*
Husam Alissa, *Microsoft, Redmond, WA*
Jenwei Liang, *MediaTek, Hsinchu, Taiwan*
David Goldston, *MIT, Washington, DC*

AI-Accelerators

Session Chair: Soojung Ryu, *Seoul National University, Seoul, Korea*
Session Co-Chair: Hugh Mair, *MediaTek, Dallas, TX*

8:00 AM

23.1 T-REX: A 68-to-567μs/Token 0.41-to-3.95μJ/Token Transformer Accelerator with Reduced External Memory Access and Enhanced Hardware Utilization in 16nm FinFET

S. Moon[1], M. Li[1], G. K. Chen[2], P. C. Knag[2], R. Krishnamurthy[2], M. Seok[1]

[1]Columbia University, New York, NY
[2]Intel, Hillsboro, OR

8:25 AM

23.2 DS2 A 28nm 0.22μJ/Token Memory-Compute-Intensity-Aware CNN-Transformer Accelerator with Hybrid-Attention-Based Layer-Fusion and Cascaded Pruning for Semantic Segmentation

P. Dong[1,2], Y. Tan*[1,2], X. Liu[2], P. Luo[2], Y. Liu[2], L. Liang[2], Y. Zhou[2], D. Pang[2], M-T. Yung[2], D. Zhang[1,2], X. Huang[1,2], S-Y. Liu[1,2], Y. Wu[1,2], F. Tian[1,2], C-Y. Tsui[1,2], F. Tu[1,2], K-T. Cheng[1,2]*

[1]Hong Kong University of Science and Technology, Hong Kong, China
[2]AI Chip Center for Emerging Smart System, Hong Kong, China
*Equally Credited Authors (ECAs)

8:50 AM

23.3 DS2 EdgeDiff: 418.4mJ/Inference Multi-Modal Few-Step Diffusion Model Accelerator with Mixed-Precision and Reordered Group Quantization

S. Kim, J. Oh, J. So, Y. Choi, S. Kim, D. Im, G. Park, H-J. Yoo

KAIST, Daejeon, Korea

9:15 AM

23.4 Nebula: A 28nm 109.8TOPS/W 3D PNN Accelerator Featuring Adaptive Partition, Multi-Skipping, and Block-Wise Aggregation

C. Zhou[1], T. Huang[1], Y. Ma[1], Y. Fu[1], X. Song[1], S. Qiu[1], J. Sun[1], M. Liu[1], G. Li[1], Y. He[2], Y. Yang[1,3], H. Jiao[1]

[1]Peking University, Shenzhen, China
[2]Reconova Technologies, Xiamen, China
[3]Peking University, Beijing, China

Break 9:40 AM

10:05 AM

23.5 MAE: A 3nm 0.168mm² 576MAC Mini Autoencoder with Line-Based Depth-First Scheduling for Generative AI in Vision on Edge Devices

S-W. Hsieh, C-H. Yuan, M-H. Lin, P-Y. Tsai, Y-Y. Nian, C-Y. Cheng, H-W. Chih, P-H. Chiang, M-H. Chiang, Y-J. Kuo, Y-W. Wu, Y-S. Chen, P-H. Chen, S. Huang, M-E. Shih, C-P. Chen, A. Chen, S. Chang, C-M. Wang, P-Y. Yeh, J. Liu, Y-C. Chang, C-Y. Chen, C-C. Ju, C. Wang, Y. K. Jou

MediaTek, Hsinchu, Taiwan

10:30 AM

23.6 MEGA.mini: A Universal Generative AI Processor with a New Big/Little Core Architecture for NPU

D. Han[1,2], A. P. Chandrakasan[1]

[1]Massachusetts Institute of Technology, Cambridge, MA
[2]Chung-Ang University, Seoul, Korea

10:55 AM

23.7 BROCA: A 52.4-to-559.2mW Mobile Social Agent System-on-Chip with Adaptive Bit-Truncate Unit and Acoustic-Cluster Bit Grouping DS2

W. Jo, S. Hong, J. Choi, B. Kwon, H. Sang, D. Im, S. Kim, S. Kim, T. Lee, H-J. Yoo

KAIST, Daejeon, Korea

11:20 AM

23.8 An 88.36TOPS/W Bit-Level-Weight-Compressed Large-Language-Model Accelerator with Cluster-Aligned INT-FP-GEMM and Bi-Dimensional Workflow Reformulation

Y. Qin, Y. Wang, J. Wang, Z. Lin, Y. Zhao, S. Wei, Y. Hu, S. Yin

Tsinghua University, Beijing, China

11:35 AM

23.9 Slim-Llama: A 4.69mW Large-Language-Model Processor with Binary/Ternary Weights for Billion-Parameter Llama Model DS2

S. Kim, J. Lee, H-J. Yoo

KAIST, Daejeon, Korea

11:50 AM

23.10 HuMoniX: A 57.3fps 12.8TFLOPS/W Text-to-Motion Processor with Inter-Iteration Output Sparsity and Inter-Frame Joint Similarity

J. Heo, A. Putra, S. Yune, J. Yoon, H. Lee, J. Kim, J-Y. Kim

KAIST, Daejeon, Korea

Conclusion 12:05 PM

High-Frequency ADCs

Session Chair: Seung-Tak Ryu, *KAIST, Daejeon, Korea*
Session Co-Chair: Vanessa Chen, *Carnegie Mellon University, Pittsburgh, PA*

8:00 AM

24.1 A 12b 3GS/s Pipelined ADC with Gated-LMS-Based Piecewise-Linear Nonlinearity Calibration

M. Gu, Y. Zhong, L. Jie, N. Sun
Tsinghua University, Beijing, China

8:25 AM

24.2 A 14b 1GS/s Single-Channel Pipelined ADC with a Parallel-Operation SAR Sub-Quantizer and a Dynamic-Deadzone Ring Amplifier

Y. Cao[1], Y. Shen[1,2], S. Liu[1,2], H. Han[1], H. Liang[1], L. Dang[1], D. Li[1], R. Ding[1,2], Z. Zhu[1,2]
[1]Xidian University, Xi'an, China
[2]Hangzhou Institute of Technology, Xidian University, Hangzhou, China

8:50 AM

24.3 A PVT-Robust 2× Interleaved 2.2GS/s ADC with Gated-CCRO-Based Quantizer Shared Across Channels and Steps Achieving >4.5GHz ERBW

J. Zhong[1], M. Zhang[1], Y. Zhu[1], R. P. Martins[1,2], C-H. Chan[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

9:15 AM

24.4 A 10b 3GS/s Time-Domain ADC with Mutually Exclusive Metastability Correction and Wide Common-Mode Input

Z. Liu[1], M. Zhang[1], W. Zhang[1], Y. Zhu[1], R. P. Martins[1,2], C-H. Chan[1]
[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 9:40 AM

10:05 AM

24.5 A 72GS/s 9b Time-Interleaved Pipeline-SAR ADC Achieving 55.3/49.3dB SFDR at 20GHz/Nyquist Inputs in 16nm FinFET

Y. Zhang[1], M. Zhang[1], Z. Wu[1], Y. Zhu[1], R. P. Martins[1,2], C-H. Chan[1]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

10:30 AM

24.6 A Power- and Area-Efficient 4nm Self-Calibrated 12b/16GS/s Hierarchical Time-Interleaving ADC

C-E. Hsieh[1], G. Manganaro*[2], S-H. Liao*[1], J. Weng*[1], T-Y. Fan[1], A. Chin[1], T-C. Hung[1], J. X. Wu[2], C-L. Lo[2], A. Pan[1], M-H. Hsieh[1], Y. Shu[1], W-H. Tseng[1], K-D. Chen[1]*

[1]MediaTek, Hsinchu, Taiwan
[2]MediaTek, Woburn, MA
*Equally Credited Authors (ECAs)

10:55 AM

24.7 An 8b 10GS/s 2-Channel Time-Interleaved Pipelined ADC with Concurrent Residue Transfer and Quantization, and Automatic Buffer Power Gating

Y. Tao, M. Zhan, M. Gu, X. He, Y. He, Z. Zhang, Y. Zhong, L. Jie, N. Sun

Tsinghua University, Beijing, China

11:20 AM

24.8 A 12GS/s 9b 16× Time-Interleaved SAR ADC in 16nm FinFET

J. Shen[1], W-H. Chen[2], E. Burlingame[3], S. Weinreich[1], M. Elliott[4], S. McCracken[1], J. Kenney[2], J. Brunsilius[3], A. Korkmaz[5], E. A. Fontecilla[3], N. Rakuljic[3], U. Mehta[3], B. Sullivan[1], J. Scuteri[5], B. B. Luu[3], M. Nichols[3], D. Martin[6], R. Sullivan[5], D. DeBolt[1], R. Kapusta[1]

[1]Analog Devices, Wilmington, MA
[2]Analog Devices, Somerset, NJ
[3]Analog Devices, San Diego, CA
[4]Analog Devices, Austin, TX
[5]Analog Devices, Durham, NC
[6]Analog Devices, Limerick, Ireland

Conclusion 11:45 AM

High Concepts at High Frequencies

Session Chair: Noriyuki Miura, *Osaka University, Suita, Japan*
Session Co-Chair: Denis Daly, *Apple, Waltham, MA*

8:00 AM

25.1 A Physics-Inspired Oscillator-Based Mixed-Signal Optimization Engine for Solving 50-Variable 218-Clause 3-SAT Problems with 100% Solvability and 31.7µs Solution Time

E. Dikopoulos, Y-T. Hsu, L. Wormald*, W. Tang, Z. Zhang, M. P. Flynn*

University of Michigan, Ann Arbor, MI
*Equally Credited Authors (ECAs)

8:25 AM

25.2 DS2 A 4GS/s Fully Analog 256×256 MP-Based Cross-Correlator with 1000TOPS/W Compute Efficiency and 1.3TOPS/mm² Compute Density in 22nm SOI CMOS

A. Undavalli[1], K. Rashed[2], G. Cauwenberghs[3], S. Chakrabartty[1], A. Natarajan[2], A. Nagulu[1,4]

[1]Washington University in St. Louis, Saint Louis, MO
[2]Oregon State University, Corvallis, OR
[3]University of California, San Diego, CA
[4]Northeastern University, Oakland, CA

8:50 AM

25.3 AI-Enabled Design Space Discovery and End-to-end Synthesis for RFICs with Reinforcement Learning and Inverse Methods Demonstrating mm-Wave/sub-THz PAs between 30 and 120GHz

J. Zhou[1], E. A. Karahan*[1], S. Ghozzy[1], Z. Liu[1,2], H. Jalili[1], K. Sengupta[1]*

[1]Princeton University, Princeton, NJ
[2]Texas Instruments, Dallas, TX
*Equally Credited Authors (ECAs)

9:15 AM

25.4 A Micromachined Heterogeneously Integrated Active-Probe Enabling Non-Disruptive In-Situ Measurements from DC to 50GHz

J. Moody, T. Liebsch, P. Finnegan, S. Lepkowski, R. Costanzo, M. Hirabayashi, M. Jordan, T. Forbes, C. Nordquist

Sandia National Laboratories, Albuquerque, NM

9:30 AM

25.5 A 99.5mW/port DC-to-40GHz Integrated Channel Analyzer for High-Density Signal Integrity Measurement in 28nm CMOS

G. Wu[1], Y. Li*[1], B. Ye*[1,2], F. Li[1], X. Liu[1], H. Niu[1], R. Wang[1], D. Yu[1], W. Gai[1,3]*

[1]Peking University, Beijing, China
[2]East China Normal University, Shanghai, China
[3]Beijing Advanced Innovation Center for Integrated Circuits, Beijing, China
*Equally Credited Authors (ECAs)

Break 9:45 AM

Wireless Transmitters and Front-Ends

Session Chair: Alireza Zolfaghari, *Broadcom, Irvine, CA*
Session Co-Chair: Giuseppe Gramegna, *imec, Leuven, Belgium*

10:05 AM

26.1 A 24GHz Direct Digital Transmitter Using Multiphase Subharmonic Switching PA Achieving 3.2Gb/s Data Rate and -30.8dB EVM in 65nm CMOS

S. Mahapatra[1], M. Ayesh[1], C. Yang[1], M. Palaria[1], S. Su[1,2], A. Zhang[3], M. S-W. Chen[1]

[1]University of Southern California, Los Angeles, CA
[2]University of Waterloo, Waterloo, Canada
[3]Tsinghua University, Beijing, China

10:30 AM

26.2 A Wideband Replicas-Rejection Digital Transmitter Using Joint-Digital-Analog Interpolation and Filtering in 28nm CMOS

C. Hu, J. Li*, J. Lin, H. Xu, Y. Yin*

Fudan University, Shanghai, China
*Equally Credited Authors (ECAs)

10:55 AM

26.3 A Crystal-less Frequency-Modulation Transmitter IC with Joint Neural-Network-Driven Modulation and Coding for Low-Power Connectivity

Y. Shen, B. Chang, C-W. Tseng, Y. Wang, Q. Zhang, Z. Fan, Z. Feng, R. Narashimha, A. Bejarano-Carbo, H-S. Kim, D. Blaauw
University of Michigan, Ann Arbor, MI

11:20 AM

26.4 A 24-to-29GHz Compact Transmit/Receive Front-End Module Featuring an Asymmetric Doherty Power Amplifier and 0.22mm² Area

X. Zhang, R. Wang*, Q. Zhou*, H. Guo, C. Shi, T. Chi*

Rice University, Houston, TX
*Equally Credited Authors (ECAs)

11:45 AM

26.5 A 17.7-to-29.5GHz Transceiver Front-End with 3.3dB NF and 20.2dBm OP1dB in 65nm CMOS

B. Yang[1], N. Li[2], Y. Liu[1], H. Lu[1], H. Gao[1], S. Wang[1], J. Xu[1], X. He[1], N. Yan[3], Q. J. Gu[4], C. Song[2], Z. Xu[1]

[1]Zhejiang University, Zhoushan, China
[2]Donghai Laboratory, Zhoushan, China
[3]Fudan University, Shanghai, China
[4]Georgia Institute of Technology, Atlanta, GA

Conclusion 12:00 PM

Sensor Interfaces

Session Chair: Caspar van Vroonhoven, *Analog Devices, Munich, Germany*
Session Co-Chair: Chinwuba Ezekwe, *Robert Bosch, Sunnyvale, CA*

8:00 AM

27.1 DS2 A 3-Axis MEMS Gyroscope with 2.8ms Wake-Up Time Enabled by a 1.5µW Always-On Drive Loop

L. Zhong[1], J. Zhang[1], C. Li[1], L. Wang[1], M. Zhong[1], K. Cai[2], J. Gao[2], T. Hu[2], Z. Zhu[1]

[1]Xidian University, Xi'an, China
[2]Silan Microelectronics, Hangzhou, China

8:25 AM

27.2 A Voltage-Biased CMOS Hall Sensor with 1.0µT (3σ) Offset and a 60nT/√Hz Noise-Floor

F. J. van Mourik[1], S. Pan[2], K. M. Dowling[1], K. A. Makinwa[1]

[1]TU Delft, Delft, The Netherlands
[2]Tsinghua University, Beijing, China

8:50 AM

27.3 A Sub-1V 14b 5.8nW/Hz BW/Power-Scalable CT Sensor Interface with a Frequency-Controlled Current Source Achieving a 225× Scalable Range

X. Wu[1], Y. Liu[2], X. Yu[1], N. N. Tan[2], Z. Tang[2]

[1]Zhejiang University, Hangzhou, China
[2]Vango Technologies, Hangzhou, China

9:15 AM

27.4 A BJT-Based Temperature Sensor with an 80fJ·K² Resolution FoM

N. G. Toth, K. A. A. Makinwa

TU Delft, Delft, The Netherlands

9:30 AM

27.5 DS2 A 4,100µm² Wire-Metal-Based Temperature Sensor with a Fractional-Discharge FLL and a Time-Domain Amplifier with ±0.2°C Inaccuracy (3σ) from –40 to 125°C and 45fJ·K² Resolution FoM in 28nm CMOS

D. Shi[1], K-M. Lei[1], R. P. Martins[1,2], P-I. Mak[1]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 9:45 AM

Capacitive Sensor Readout

Session Chair: Caspar van Vroonhoven, *Analog Devices, Munich, Germany*
Session Co-Chair: Chinwuba Ezekwe, *Robert Bosch, Sunnyvale, CA*

10:05 AM

28.1 An 18.5nF-Input-Range PM-SAR-Hybrid Capacitance-to-Digital Converter Achieving 6.1µs Conversion Time at 18.1pF Input Capacitance

D. Youn[1], K. Jeong[2], W. Youn[1], H. Seong[1], Y. Park[1], S. Ha[3], M. Je[1]
[1]KAIST, Daejeon, Korea
[2]ETH Zürich, Zürich, Switzerland
[3]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

10:30 AM

28.2 A 189.3dB-FoM$_S$ 14.5fJ/Conversion-Step Continuous-Time Noise-Shaping SAR Capacitance-to-Digital Converter

G. Yun[1], H. Choi[1], Y. Jung[1,2], J. Myung[1], S. Oh[1], S. Ha[3], M. Je[1]
[1]KAIST, Daejeon, Korea
[2]*now at imec, Leuven, Belgium
[3]New York University Abu Dhabi, Abu Dhabi, United Arab Emirates

10:55 AM

28.3 A 185.2dB-FoM$_s$ 8.7aF$_{rms}$ Zoomed Capacitance-to-Digital Converter with Chopping-Based kT/C Noise Cancellation and Add-Then-Subtract Phase-Domain Lead-Compensation Technique

B. Li, Z. Shen, H. Luo, J. Yang, Z. Wang, Y. Wang, X. Tang
Peking University, Beijing, China

11:20 AM

28.4 A 143dB-Dynamic-Range 119dB-CMRR Capacitance-to-Digital Converter for High-Resolution Floating-Target Displacement Sensing

S. Pan[1], X. Zhang[1], B. Zheng[1], Y. Cheng[1], H. Jiang[2], H. Wu[1]
[1]Tsinghua University, Beijing, China
[2]CoSensing, Utrecht, The Netherlands

Conclusion 11:45 AM

SRAM

Session Chair: John Wuu, *Advanced Micro Devices, Fort Collins, CO*
Session Co-Chair: Eric Wang, *TSMC, Hsinchu, Taiwan*

8:00 AM

29.1 A 38.1Mb/mm² SRAM in a 2nm-CMOS-Nanosheet Technology for High-Density and Energy-Efficient Compute

T-Y. J. Chang, Y-H. Chen, K. V. Reddy, N. Puri, T. Masina, K-C. Lin, P-S. Wang, Y. Lin, C-Y. Lin, Y-H. Nien, H. Fujiwara, K-F. Lin, M-H. Chang, C. W. Wu, R. Lee, Y. Wang, H-J. Liao, Q. Li, P. W. Wang, G. Yeap

TSMC, Hsinchu, Taiwan

8:25 AM

29.2 A 0.021µm² High-Density SRAM in Intel-18A-RibbonFET Technology with PowerVia-Backside Power Delivery

X. Wang[1], Y. Kim[1], G. H. Baek[1], K. G. Bannore[1], K. Dave[1], A. Joushaghani[1], N. Kang[1], M. Ko[1], A. Mahadevan Pillai[2], H. C. P. Movva[1], G. Park[1], M. Rahman[1], S. Subramaniam[1], V. Vashishtha[1], T. Yang[1], Z. Guo[1], E. A. Karl[1]

[1]Intel, Hillsboro, OR

[2]Intel, Santa Clara, CA

8:50 AM

29.3 A 3nm FinFET 2.2Gsearch/s 0.305fJ/b TCAM with Dynamically Gated Search Lines for Data-Center ASICs

S. Kumar[*1], G. Jedhe*[*1], C. Deshpande*[*1], A. Gogoi[1], P. Su[2], K. S. Jway[3], T. Seoh[3]*

[1]MediaTek, San Jose, CA
[2]MediaTek, Hsinchu, Taiwan
[3]MediaTek, Singapore, Singapore
*Equally Credited Authors (ECAs)

9:15 AM

29.4 DS2 A 38Mb/mm² 380/540mV Dual-Rail SRAM in 3nm-FinFET Technology

H. Pilo[1], J. Barth[1], K. D. Dwivedi[2], P. Lee[3], V. Kumar[2], P. Nalawar[4], Y. Patel[2], S. Sharad[2], S. Singh[2]

[1]Synopsys, Williston, VT
[2]Synopsys, Noida, India
[3]Synopsys, Sunnyvale, CA
[4]Synopsys, Bangalore, India

9:30 AM

29.5 A 3nm 3.6GHz Dual-Port SRAM with Backend-RC Optimization and a Far-End Write-Assist Scheme

H. Fujiwara[1], W-C. Zhao[1], K. Khare[1], Y-H. Nien[1], C-Y. Lin[1], C-H. Lin[1], S-R. Liao[1], K. Torigoe[2], S. Xia[3], Y. Ishii[3], Y-Y. Liu[1], J-J. Liaw[1], Y-H. Chen[1], H-J. Liao[1], T-Y. J. Chang[1]

[1]TSMC, Hsinchu, Taiwan
[2]TSMC Design Technology Japan, Osaka, Japan
[3]TSMC Design Technology Japan, Yokohama, Japan

Break 9:45 AM

Nonvolatile Memory and DRAM

Session Chair: Seung-Jae Lee, *Samsung Electronics, Gyeonggi, Korea*
Session Co-Chair: Thomas Hein, *Micron, Munich, Germany*

10:05 AM

30.1 A 28Gb/mm² 4XX-Layer 1Tb 3b/cell WF-Bonding 3D-NAND Flash with 5.6Gb/s/pin IOs

S-S. Park, J-D. Lyu, M. Kim, J. Lee, Y. Song, C-H. Yu, H. Makoto, Y. Kwon, J-H. Park, H-J. Kim, D. Lee, D. Seo, B. Go, S. Jeon, Y. Kim, D-H. Kim, Y. Jo, H. Yoon, J. Park, I. Kim, S. Kim, H. Lee, J-H. Yu, S-L. Kim, H-S. Ku, J. Seo, J. Byun, S-H. Yun, K. Kang, S-B. Kim, Y. Lee, Y. Lee, K. Kang, H-J. Lee, Y. Ryu, H. Kim , W. Kim, H. Choi, J. Jeon, A. Park, R. Song, J-H. Kim, J-S. Kim, H-S. Lee, M-K. Lee, J-I. Son, J. Cho, M. Kim, J-W. Im, J. Park, H. Kwon, Y. Choi, C. Yoon, S. Lee, K. Song, S-H. Hur
Samsung Electronics, Hwaseong, Korea

10:30 AM

30.2 A 1Tb 3b/cell 3D-Flash Memory with a 29%-Improved-Energy-Efficiency Read Operation and 4.8Gb/s Power-Isolated Low-Tapped-Termination IOs

K. Yanagidaira[1], M. Sako[1], Y. Hirashima[1], J. Matsuno[1], Y. Higashi[1], Y. Shimizu[1], A. Imamoto[1], K. Kawaguchi[1], K. Tabata[1], T. Nakano[1], Y. Ochi[1], H. Hoshino[1], T. Hioka[1], S. Saigusa[1], H. Date[1], M. Unno[1], J. Sato[1], Y. Kamata[1], H. Chibvongodze[2], N. Ojima[2], H. Sugawara[2], M. Kano[2], J-W. Lee[2], H. Mizukoshi[2], R. Yamashita[2], K. Abe[2], N. Morozumi[2], I-S. Yoon[2], T. Ariki[2], J. H. Yuh[2], K. Htoo[2], Y. Kato[2], Y. Watanabe[1], T. Kouchi[1], [1]KIOXIA, Tokyo, Japan; [2]Western Digital, Milpitas, CA

10:55 AM

30.3 A 24Gb 42.5Gb/s GDDR7 DRAM with Low-Power-WCK Distribution, an RC-Optimized Dual-Emphasis TX, and Voltage/Time-Margin-Enhanced Power Reduction

S-H. Kim, J. Baek, M-C. Choi, D. Lee, D. An, S. M. Kim, Y. Song, M. Shim, S-Y. Cho, D. Lee, G. Cho, I-W. Jun, J. Park, T. Lee, H-C. Jung, C. Lee, G-Y. Kang, H-R. Kim, J. Lee, Y. S. Joo, H-J. Jung, B. Won, J-H. Yu, S. Han, Y. Hwang, C. Kim, S-J. Kim, Y. Lee, Y-T. Kim, M-O. Kim, W. Shin, T-Y. Oh, S. Hwang
Samsung Electronics, Hwaseong, Korea

11:20 AM

30.4 A 16Gb 12.7Gb/s/pin LPDDR5-Ultra-Pro DRAM with 4-Phase Self-Calibration and AC-Coupled Transceiver Equalization in a 5th-Generation 10nm DRAM Process

J-H. Baek, J-H. Kim, Y-C. Sung, J-W. Jeong, J-K. Park, H-K. Oh, B-H. Lee, D-W. Ko, T-S. Oh, S-G. Hong, C-K. Kwon, D. Lim, M-O. Kim, S-J. Bae, T-Y. Oh, S-J. Hwang
Samsung Electronics, Hwaseong, Korea

11:35 AM

30.5 A 321-Layer 2Tb 4b/cell 3D-NAND-Flash Memory with a 75MB/s Program Throughput

W. Cho[1], C. Jeong[1], J. Kim[1], J. Jung[1], K. Ahn[1], J. Goo[1], S. Lee[1], K. Cho[1], T. Cho[1], D. Kim[1], G. Park[1], Y. Ahn[1], S. Chai[1], G. Ko[1], S. Jung[1], E. Jo[1], T. Park[1], J. Ban[1], C. Park[1], J. H. Park[1], S. Oh[1], S. Jeong[1], Y. Kwak[1], K. Jeong[1], J. Kim[1], M. Shin[1], E. Yang[1], T. Shin[1], Y. Kim[1], J. Mun[1], C. Ryu[1], H. Park[1], C. Ha[2], J. T. Park[2], P. Zhang[3], S. Park[2], R. Haque[3], H. Tian[2], S. Ok[1], W. Choi[1], J. Lim[1], D. Yoon[1], S. Park[1], W. Park[1], K. Gwon[1], S. Lee[1], H. Huh[1], W. Jeong[1], J. Choi[1]
[1]SK hynix, Icheon, Korea; [2]SK hynix, San Jose, CA; [3]SK hynix, Rancho Cordova, CA

11:50 AM

30.6 A 64Gb DDR4 STT-MRAM Using a Time-Controlled Discharge-Reading Scheme Using a 0.001681µm² 1T-1MTJ Cross-Point Cell

K. Hatsuda[1], K. Hoya[1], R. Takizawa[1], F. Matsuoka[1], T. Yasuda[1], A. Katayama[1], T. Miyakawa[1], K. Senju[1], K. Okawa[1], Y. Furukawa[1], Y. Shimada[1], K. Kotake[1], S. Hirokawa[1], M. C. Shin[2], D. K. Kim[2], T. H. Kim[2], K. Kim[2], H. Aikawa[3], J. Song[2], T. Nagase[3], S. M. Seo[2], S. G. Kim[2], S. Y. Cha[2]
[1]KIOXIA, Yokohama, Japan; [2]SK hynix, Icheon, Korea; [3]KIOXIA Korea, Seoul, Korea

Conclusion 12:05 PM

Energy Harvesting and IoT Power

Session Chair: Gael Pillonnet, *CEA-Leti, Grenoble, France*
Session Co-Chair: Sung-Wan Hong, *Sogang University, Seoul, Korea*

1:30 PM

31.1 An Inductor-less Capacitor-less Synchronous Piezoelectric-Electromagnetic Hybrid Energy Harvesting Platform with Coil-Sharing Scheme

Y. Wei[*1], *X. Yue*[*1], *Z. Chen*[2], *S. Du*[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Fudan University, Shanghai, China
*Equally Credited Authors (ECAs)

1:55 PM

31.2 A Biased-SECE Interface for Piezoelectric Energy Harvesting with Geometric-Mean-Computational MPPT Achieving 99.9% MPPT Efficiency, 8.75Cycles/ΔV_{OC} Tracking, and 9.3× Energy Extraction

J. Lee, H-S. Kim

KAIST, Daejeon, Korea

2:20 PM

31.3 A Rectifier-less Piezoelectric Energy-Harvesting Interface with a Sense & Track MPPT Achieving Single-Cycle Convergence and 568% Shock Power Improvement

S. Jiang[*1], *X. Yue*[*1], *Y. Ma*[1], *C. Wang*[2], *S. Du*[1]

[1]Delft University of Technology, Delft, The Netherlands
[2]Huazhong University of Science and Technology, Wuhan, China
*Equally Credited Authors (ECAs)

2:45 PM

31.4 A 91.25% Peak-Power-Conversion-Efficiency Capacitive Power-Management IC Supporting up to 5.68mJ Burst Energy Delivery Using a Single External Capacitor for mm-Scale IoT Applications

Q. Fang[1], *F. Li*[1], *R. P. Martins*[1,2], *M-K. Law*[1]

[1]University of Macau, Macau, China
[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

Break 3:10 PM

Isolated Power and Gate Drivers

Session Chair: Lin Cheng, *University of Science and Technology of China, Hefei, China*

Session Co-Chair: Shusuke Kawai, *Toshiba , Kawasaki, Japan*

3:35 PM

32.1 A 180MHz 45.3%-Peak-Efficiency Isolated Converter Using Q-Downsize Class-D Power Amplifier with Inherent Shoot-Through Current Blocking and High Tolerance for Efficiency Despite Frequency Misalignments

T. Xia[1], Q. Chen*[1], S. Wang[1], R. P. Martins[1,2], M. Huang[1]*

[1]University of Macau, Macau, China

[2]Instituto Superior Tecnico/University of Lisboa, Lisbon, Portugal

*Equally Credited Authors (ECAs)

4:00 PM

32.2 A Single-Link Multi-Domain-Output (SLiMDO) Isolated DC-DC Converter with Passive Magnetic Flux Sharing for Local Energy Distribution and RX Behavior Sensing-Based Global Power Modulation

J. Jiang, L. Zhao, J. Tang, C. Huang, Iowa State University, Ames, IA

4:25 PM

32.3 An Accurate Secondary-Side Controller with GaN-Based C_{GS} Isolated Driver Achieving Sub-1% Error On-Chip Sensing

C-Y. Chen[1], T-W. Wang[1], P-J. Chiu[1], Y-T. Huang[1], X-Q. Wu[1], C-W. Cho[1], S-H. Hung[1], Y-T. Shih[1], K-H. Chen[1], K-L. Zheng[2], Y-H. Lin[3], S-R. Lin[3], T-Y. Tsai[3], H-H. Tsai[4]

[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan

[2]Chip-GaN Power Semiconductor, Hsinchu, Taiwan

[3]Realtek Semiconductor, Hsinchu, Taiwan

[4]Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

4:50 PM

32.4 A Dual-LC-Resonant Isolated DC-DC Converter Achieving 65.4% Peak Efficiency and Inherent Backscattering

Q. Huang, D. Pan*, Z. Chen, L. Cheng*

University of Science and Technology of China, Hefei, China

*Equally Credited Authors (ECAs)

5:05 PM

32.5 A 2W 53.2%-Peak-Efficiency Multi-Core Isolated DC-DC Converter with Embedded Magnetic-Core Transformer Achieving CISPR-32 Class-B EMI Compliance and <5mV Ripple

D. Pan[1], W. Xu[2], L. Zhang[1], Q. Huang[1], L. Cheng[1,2]

[1]University of Science and Technology of China, Hefei, China

[2]Hefei CLT Microelectronics, Hefei, China

5:20 PM

32.6 A Dynamic-R_{ON}-Diminished Bidirectional GaN Load Switch with Inrush Current Protection and Spike Attenuation

P-J. Chiu[1], T-W. Wang[1], X-Q. Wu[1], C-Y. Chen[1], Y-T. Huang[1], C-W. Cho[1], S-H. Hung[1], Y-T. Shih[1], K-H. Chen[1], K-L. Zheng[2], Y-H. Lin[3], S-R. Lin[3], T-Y. Tsai[3], H-H. Tsai[4]

[1]National Yang Ming Chiao Tung University, Hsinchu, Taiwan

[2]Chip-GaN Power Semiconductor, Hsinchu, Taiwan

[3]Realtek Semiconductor, Hsinchu, Taiwan

[4]Taiwan Semiconductor Research Institute, Hsinchu, Taiwan

Conclusion 5:35 PM

Components for Beyond 100GHz

Session Chair: Jeremy Dunworth, *Qualcomm Technologies, La Jolla, CA*
Session Co-Chair: Hiroshi Hamada, *NTT, Atsugi, Japan*
Session Co-Chair: Mona Hella*, *Rensselaer Polytechnic Institute, Troy, NY*

1:30 PM

33.1 A 232-to-260GHz CMOS Amplifier-Multiplier Chain with a Low-Cost, Matching-Sheet-Assisted Radiation Package and 11.1dBm Total Radiated Power

J. Wang, D. Sheen, X. Chen, S. F. Nagle, R. Han
Massachusetts Institute of Technology, Cambridge, MA

1:55 PM

33.2 A 216-to-226GHz Watt-Level GaN Solid-State Power Amplifier with Multiband Large-Signal Impedance Correction and Circuit-Package Co-Design Technique

W. Wang[1,2], Z. Li*[3], K. Li[3], H. Cheng[1,2], F. Guo[1,2], Y. Zhang[1,2], K. Wang[3]*
[1]National Key Laboratory of Solid-State Microwave Devices and Circuits, Nanjing, China
[2]Nanjing Electronic Device Institute, Nanjing, China
[3]Tianjin University, Tianjin, China
*Equally Credited Authors (ECAs)

2:20 PM

33.3 A 125-to-170GHz Power-Efficient Phase Shifter in SiGe BiCMOS with Outphasing Gain and Phase Corrections

L. Piotto, G. De Filippi, A. Mazzanti
University of Pavia, Pavia, Italy

2:45 PM

33.4 A Wideband Bidirectional Calibration-Free Frequency/Switching-Staggering 360° D-Band Phase Shifter with Frequency-Invariant Codes Achieving <2.38°/0.63dB RMS-Errors Over 24% Bandwidth

B. A. Abdelmagid, Y. Liu, H. Wang
ETH Zürich, Zürich, Switzerland

3:00 PM

33.5 A 224GHz 19.9% TR Varactor-less VCO Utilizing a Multi-Section Switch-Loaded Coupled-Line Resonator

A. Elmenshawi[1], S. Muralidharan[2], M. M. Hella[1]
[1]Rensselaer Polytechnic Institute, Troy, NY
[2]Analog Devices, Beaverton, OR

Break 3:15 PM

**1971 to 2025*

Digital PLLs and Waveform-Shaping VCOs

Session Chair: Xiang Gao, *Zhejiang University, Hangzhou, China*
Session Co-Chair: Yu-Li Hsueh, *Mediatek, Hsinchu, Taiwan*

3:35 PM

34.1 A 65fs$_{rms}$-Jitter and -272dB-FoM$_{jitter,N}$ 10.1GHz Fractional-N Digital PLL with a Quantization-Error-Compensating BBPD and an Orthogonal-Polynomial LMS Calibration

M. Chae[1], S. Jang*[1], C. Hwang[1,2], H. Park[1,2], J. Choi[1]*

[1]Seoul National University, Seoul, Korea; [2]KAIST, Daejeon, Korea
*Equally Credited Authors (ECAs)

4:00 PM

34.2 A 380µW and -242.8dB FoM Digital-PLL-Based GFSK Modulator with sub-20µs Settling Frequency Hopping for Bluetooth Low-Energy in 22nm CMOS

S. M. Dartizio[1], G. Castoro*[1], S. Gallucci*[1], M. Rossoni[1], R. Moleri[1], F. Tesolin[1], P. Salvi[1], S. Karman[2], A. L. Lacaita[1], S. Levantino[1]*

[1]Politecnico di Milano, Milan, Italy; [2]Infineon Technologies, Villach, Austria
*Equally Credited Authors (ECAs)

4:25 PM

34.3 A 4.75GHz Digital PLL with 45.8fs Integrated-Jitter and 257dB FoM Based on a Voltage-Biased Harmonic-Shaping DCO with Adaptive Common-Mode Resonance Tuning

S. Gallucci[1], F. Tesolin*[1], P. Salvi[1], D. Lodi Rizzini[1], R. Moleri[1], F. Buccoleri[1,2], M. Rossoni[1], G. Castoro[1], S. M. Dartizio[1], C. Samori[1], A. L. Lacaita[1], S. Levantino[1]*

[1]Politecnico di Milano, Milan, Italy
[2]now with Kandou Bus SA, Saint-Sulpice, Switzerland
*Equally Credited Authors (ECAs)

4:50 PM

34.4 A 9.05-to-37.0GHz LO Generator with Magnetic Mode Switching and Tuning-Free Octave-Bandwidth Common-Mode Resonator Achieving >190.7dBc/Hz FoM

H. Guo, Y. Hu, T. Chi, Rice University, Houston, TX

5:05 PM

34.5 An 18.5-to-23.6GHz Quad-Core Class-F_{23} Oscillator Without 2nd/3rd Harmonic Tuning Achieving 193dBc/Hz Peak FoM and 140-to-250kHz 1/f^3 PN Corner in 65nm CMOS

H. Cao[1], S. Gao*[1], J. Jin[1], X. Liu[2], W. Wu[1], T. Huang[1]*

[1]Nanjing University of Science and Technology, Nanjing, China
[2]Southern University of Science and Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

5:20 PM

34.6 A 47.3-to-58.4GHz Differential Quasi-Class-E Colpitts Oscillator Achieving 198.8dBc/Hz FoM$_T$

C. Song, Z. Kang*, C. Yu, L. Wu*

Chinese University of Hong Kong, Shenzhen, China
*Equally Credited Authors (ECAs)

Conclusion 5:35 PM

Implantable and Wearable Biomedical Devices

Session Chair: Mehdi Kiani, *Pennsylvania State University, University Park, PA*
Session Co-Chair: Bo Zhao, *Zhejiang University, Hangzhou, China*

1:30 PM

35.1 A Single-Inductor-Based High-Voltage Transmit Beamformer for Wearable Ultrasound Devices Achieving 88% fCV² Power Reduction

P. Guo, Z-Y. Chang, M. A. P. Pertijs, T. L. Costa
Delft University of Technology, Delft, The Netherlands

1:55 PM

35.2 A Spatial-Domain Compressive-Sensing Photoacoustic Imager with Matrix-Multiplying SAR ADC

H-C. Liao, S. Zhang*, Y. Su, A. Govinday, Y. Zou, W. Wang, V. Boominathan, A. Veeraraghavan, L. Li, K. Yang*
Rice University, Houston, TX
*Equally Credited Authors (ECAs)

2:20 PM

35.3 A 30MHz Wideband 92.7dB SNR 99.6% Accuracy Bioimpedance Spectroscopy IC Using Time-to-Digital Demodulation with Co-Prime Delay Locked Sampling

J. Li, D. Jiang, Y. Wu, A. Demosthenous
University College London, London, United Kingdom

2:45 PM

35.4 A Miniature Biomedical Implant Secured by Two-Factor Authentication with Emergency Access

W. Wang, Y. Su*, H-C. Liao, Y. Zou, T. Qiu, K. Yang*
Rice University, Houston, TX
*Equally Credited Authors (ECAs)

Break 3:10 PM

3:35 PM

35.5 A Wireless Adiabatic Stimulator System with Current-Mode Power Reception and Stimulus Current Regulation Achieving Precise Charge Delivery and Electrode Scalability for Miniaturized Electroceuticals

Y. Park, C. Kim, M. Je
KAIST, Daejeon, Korea

4:00 PM

35.6 An Enhanced-Frequency-Splitting-Based Wireless Power and Data Transfer System Achieving 60.2% End-to-End Efficiency and 1Mb/s Data Rate with a Sub-cm RX Coil for Miniaturized Implants

Y. Park[1], P. D. Hung[2], D. Youn[1], D. Kwon[1], C. Kim[1], M. Je[1]
[1]KAIST, Daejeon, Korea
[2]Samsung Electronics, Hwaseong, Korea

4:25 PM

35.7 A Programming-Free Three-Dimensional Resonant Current-Mode Wireless Receiver with Real-Time Link-Adaptivity and a 0.904cm^3 Receiver Coil for Implantable Systems

J-H. Kim, S-J. Lee, Y-W. Jeong, M-J. Cho, M-S. Kim, M-H. Kim, S-U. Shin
Pohang University of Science and Technology, Pohang, Korea

4:50 PM

35.8 DustNet: A Network of Time-Division Multiplexed Ultrasonic Implants with 16-Level ASK Backscatter Modulation

C. Lee, J. Pinkenburg*, M. M. Ghanbari*, C. Yalcin, M. Montalban, R. Muller*
University of California, Berkeley, CA
*Equally Credited Authors (ECAs)

Conclusion 5:15 PM

Ultra-High-Density D2D and High-Performance Optical Transceivers

Session Chair: Masum Hossain, *Carleton University, Ottawa, Canada*
Session Co-Chair: Tamer Ali, *Mediatek, Irvine, CA*

1:30 PM

36.1 A 32Gb/s 10.5Tb/s/mm 0.6pJ/b UCIe-Compliant Low-Latency Interface in 3nm Featuring Matched-Delay for Dynamic Clock Gating

M-S. Lin[1], C-C. Tsai[1], S. Li[2], W-C. Chen[1], W-H. Huang[1], Y-C. Chen[1], Y-J. Huang[1], A. Drake[3], C-H. Wen[1], P. Ranucci[3], H-H. Kuo[1], A. Yin[3], S-C. Yang[1], F. Mahmoudi[3], H-T. Ke[1], C-C. Li[1], N-C. Cheng[1], J. Wang[4], K. Lin[1], H. Liao[4], J-R. Huang[1], M-H. Wu[4], K-H. Hsieh[1], N. Amatruda[5], W. Polanco[5], D. King[5], T. Basso[6], A. Kashem[6]

[1]TSMC, Hsinchu, Taiwan
[2]TSMC, San Jose, CA
[3]TSMC, Austin, TX
[4]TSMC, Nanjing, China
[5]AMD, Austin, TX
[6]AMD, San Jose, CA

1:55 PM

36.2 A 64Gb/s/wire 10.5Tb/s/mm/layer Single-Ended Simultaneous Bi-Directional Transceiver with Echo and Crosstalk Cancellation for a Die-to-Die Interface in 28nm CMOS

Z. Wang[1], Z. Huang[1], T. Ye[1], B. Ye[2], F. Li[1], W. Wang[1,3], D. Yu[1], W. Gai[1,3]

[1]Peking University, Beijing, China
[2]East China Normal University, Shanghai, China
[3]Beijing Advanced Innovation Center for Integrated Circuits, Beijing, China

2:20 PM

36.3 A 0.29pJ/b 5.27Tb/s/mm UCIe Advanced Package Link in 3nm FinFET with 2.5D CoWoS Packaging

DS2

D. Turker Melek[1], R. NavinKumar[2], J. Vandersand[3], P. Sarkar[2], P. BS[2], A. Leuciuc[4], K. Geary[5], S. Ma[1], C. M. Mehta[1], B. Bothra[2], S. Jain[2], P. Sabharwal[6], R. Vaish[1], K. Bhanushali[3], Y. Ding[7], C. Frost[4], J. Annunziata[4], K. Sadhu[6], D. Kyritsis[5], J. Bostak[1], M. Li[7], S. Williams[4], K. Chang[8]

[1]Cadence, San Jose, CA
[2]Cadence, Bangalore, India
[3]Cadence, Cary, NC
[4]Cadence, Columbia, MD
[5]Cadence, Cork, Ireland
[6]Cadence, Noida, India
[7]Cadence, Nanjing, China
[8]now with Marvell, Santa Clara, CA

2:45 PM

36.4 A 0.9pJ/b 108Gb/s PAM-4 VCSEL-Based Direct-Drive Optical Engine

S. Krishnamurthy, S. Mondal*, J. Qiu, T. Acikalin, S. Bose, S. Yamada, J. Jaussi, M. Mansuri*

Intel, Hillsboro, OR
*Equally Credited Authors (ECAs)

Break 3:10 PM

3:35 PM

36.5 A Low-Latency 200Gb/s PAM-4 Heterogeneous Transceiver in 0.13µm SiGe BiCMOS and 28nm CMOS for Retimed Pluggable Optics

R. Tang, K. Wang*, S. Xiang, Y. Su, C. Cao, Y. He, X. Gui*

Xi'an JiaoTong University, Xi'an, China
*Equally Credited Authors (ECAs)

4:00 PM

36.6 A 112Gb/s 0.61pJ/b PAM-4 Linear TIA Supporting Extended PD-TIA Reach in 28nm CMOS

Y. Zhang, Z. Yao*, W. Zhou*, X. Luo, Z. Li, D. Zhan, Q. Pan*

Southern University of Science and Technology, Shenzhen, China
*Equally Credited Authors (ECAs)

4:25 PM

36.7 A 1.54pJ/b 64Gb/s 16-QAM Intradyne Coherent Optical Receiver in 28nm CMOS

A. E. Abdelrahman, M. B. Younis, M. O. Selim, M. S. Aly, M. A. Khalil, P. K. Hanumolu

University of Illinois, Urbana, IL

4:50 PM

36.8 A 100Gbaud 4V_{ppd} Distributed Linear Driver with Cross-Folded Transmission Lines and Cross-Coupled Gm Cells for Built-In 5-Tap FFE in 0.13µm SiGe BiCMOS

F. Chen[1,2], C. P. Yue[2], Q. Pan[1]

[1]Southern University of Science and Technology, Shenzhen, China
[2]Hong Kong University of Science and Technology, Hong Kong, China

5:15 PM

36.9 A 212Gb/s PAM-4 Retimer with Integrated High-Swing Optical Driver and Chip-to-Module Long Reach Capability of 40dB in 5nm FinFET

V. Gurumoorthy[1], A. Tan[1], A. Iyer[1], A. Fan[2], A. Farhoodfar[1], B. Alnabulsi[3], B. Helal[1], C. Abidin[2], C. Loi[4], D. Cartina[5], H. Lo[1], I. Fabiano[6], J. Riani[1], J. H. Teo[4], J. Q. Wang[1], K. Raviprakash[1], K. K. Ravi Prakash[1], L. Cai[4], L. Patra[1], M. Bachu[1], N. Codega[6], N. Shivashankar[1], S. Ray[1], S. Chong[4], S. Jafarlou[2], S. Yu[4], T-F. Wu[2], W. Y. Neo[4], X. Ding[4], Y. Wang[4], Z. Yan[1], Z. Sun[4], S. Jantzi[2], L. Tse[1], K. Chang[1]

[1]Marvell, Santa Clara, CA
[2]Marvell, Irvine, CA
[3]Marvell, Ottawa, Canada
[4]Marvell, Singapore, Singapore
[5]Marvell, Burnaby, Canada
[6]Marvell, Pavia, Italy

Conclusion 5:30 PM

Design-Technology Optimization and Digital Accelerators

Session Chair: Jae-sun Seo, *Cornell Tech, New York, NY*
Session Co-Chair: Mahmut Ersin Sinangil, *Nvidia, Santa Clara, CA*

1:30 PM

37.1 IBM Telum II Processor Design-Technology Co-Optimizations for Power, Performance, Area, and Reliability

D. Wolpert[1], G. Strevig[2], C. Berry[1], L. Sigal[3], B. Huott[1], M. Cichanowski[2], M. Pflanz[4], T. Werner[4], P. Salz[4], N. Jing[1], M. Romain[1], I. Leefken[4], R. Serton[1], R. Veerabhadraiah[5], D. Chidambarrao[3], R. Arelt[1], M. Angyal[1], B. Trombley[1], A. Haran[2], S. Hougardy[6], B. Klotz[6], R. Rao[5]

[1]IBM, Poughkeepsie, NY
[2]IBM, Austin, TX
[3]IBM, Yorktown Heights, NY
[4]IBM, Böblingen, Germany
[5]IBM, Bangalore, India
[6]University of Bonn, Bonn, Germany

1:55 PM

37.2 DS2 A 2-Dimensional mm-Scale Network-on-Textiles (kNOTs) for Wearable Computing with Direct Die-to-Yarn Integration of 0.6×2.15mm² SoC and bySPI Chiplets

A. Agrawal[1], Z. Chen[1], B. E. Desman[1], J. Wang[1], A. Tanaka[1], F. Foysal[1], C. D. Hess[1], W. Farrell[2], J. Owens[2], D. S. Truesdell[1], B. H. Calhoun[1]

[1]University of Virginia, Charlottesville, VA
[2]Nautilus Defense LLC, Pawtucket, RI

2:20 PM

37.3 Monolithic In-Memory Computing Microprocessor for End-to-End DNN Inferencing in MRAM-Embedded 28nm CMOS Technology with 1.1Mb Weight Storage

S. Kwon[1,2], S. Myung[1], J. An[1], H. Kim[1], M. Kim[1], H. Lee[1], W. Yi[1], S. Jung[1], D. Yoon[1], S. Han[3], S. Chung[3], K. Lee[3], J-H. Park[3], K. Lee[3], S. J. Kim[1], D. Ham[1,4]

[1]Samsung Advanced Institute of Technology, Suwon, Korea
[2]Seoul National University, Seoul, Korea
[3]Samsung Electronics, Giheung, Korea
[4]Harvard University, Cambridge, MA

2:45 PM

37.4 DS2 SHINSAI: A 586mm² Reusable Active TSV Interposer with Programmable Interconnect Fabric and 512Mb 3D Underdeck Memory

B. Jiao[1], H. Zhu*[1], Y. Zeng[1], Y. Li[1], J. Liao[1], S. Jia[1], Z. Chen[1], M. Tian[2], J. Zhu[2], D. Wen[2], Y. Wang[2], Y. Wang[2], J. Xu[2], F. Wang[2], J. Tao[1], C. Chen[1], Q. Liu[1], M. Liu[1]*

[1]Fudan University, Shanghai, China
[2]Kiwimoore Semiconductors, Shanghai, China
*Equally Credited Authors (ECAs)

Break 3:10 PM

3:35 PM

37.5 SKADI: A 28nm Complete K-SAT Solver Featuring Dual-Path SRAM-Based Macro and Incremental Update with 100% Solvability

Z. Wu, X. Tang, T. Zhang, L. Lin, H. Luo, B. Xu, Z. Wu, J. Song, Y. Liang, X. Bo, Y. Wang

Peking University, Beijing, China

4:00 PM

37.6 A 22nm 60.81TFLOPS/W Diffusion Accelerator with Bandwidth-Aware Memory Partition and BL-Segmented Compute-in-Memory for Efficient Multi-Task Content Generation

Y. Jing[1], J. Zhou[1], Y. Sun[1], S. He[1], P. Chen[2,3], R. Huang[1], L. Ye[1,2], T. Jia[1]

[1]Peking University, Beijing, China
[2]Advanced Institute of Information Tecnhology of Peking University, Hangzhou, China
[3]Nano Core Chip Electronic Technology, Hangzhou, China

4:25 PM

37.7 DS2 A 28nm 18.1μJ/Acquisition End-to-End GPS Acquisition Accelerator with Energy-Accuracy-Driven Mixed-Radix IFFT and ROM-Assisted Computing

S. Jeong[1], S. Park[1], M. Seok[2], D. Jeon[1]

[1]Seoul National University, Seoul, Korea
[2]Columbia University, New York, NY

4:50 PM

37.8 A 13.5μW 35-Keyword End-to-End Keyword Spotting System Featuring Personalized On-Chip Training in 28nm CMOS

H-J. Lee[1], K. Pyo[1], T. Jang[2], M. Seok[3], S. Cho[1]

[1]KAIST, Daejeon, Korea
[2]ETH Zürich, Zürich, Switzerland
[3]Columbia University, New York, NY

Conclusion 5:15 PM

FORUM 3

It's all About Data: Building Blocks, Compute, Movement and Integration

Organizers:
Yvain Thonnart, *CEA-List, Grenoble, France*
Violante Moschiano, *OpenChip Technologies, Barcelona, Spain*

Co-Organizers:
Jie Gu, *Northwestern University, Evanston, IL*
Sanu Mathew, *Intel, Hillsboro, OR*

Champions:
Fatih Hamzaoglu, *Intel, Hillsboro, OR*
Tanay Karnik, *Intel, Hillsboro, OR*

As ML is booming from huge generative AI models to mobile devices and wearables, an increasing demand for higher efficiency and performance of neural-network computing chips drives designers to optimize neural processing units and dedicated accelerators. One of the most critical challenges is the physical barrier that limits how fast data can be moved between the system, processor, and memory. This forum presents the current and next-generation circuits, architectures to improve the AI data elaboration. Starting from a software point of view of data orchestration, this forum explores trends in data-centric architecture design across different use cases for high-performance & low-power AI acceleration, in-memory computing & integration with emerging memories, and high-speed communication. The forum welcomes experts across the industry and research and will present future innovations to overcome the Memory Wall.

Thursday, February 20th, 8:00 AM

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Yvain Thonnart,** *CEA-List, Grenoble, France*
8:25 AM	**Dataflow: Is it all About Algorithms and Application Targets?** **Osman Sabri Unsal,** *BSC, Barcelona, Spain*
9:15 AM	**Dataflow Optimization and Data Sparsity Management for ML Accelerators** **Marian Verhelst,** *KU Leuven, Heverlee, Belgium*
10:05 AM	Break
10:20 AM	**Explicit Decoupled Data Orchestration: A Fundamental Approach to Acceleration** **Michael Pellauer,** *NVIDIA, Westford, MA*
11:10 AM	**Memory Solutions for AI Era: High-Bandwidth Memories and Dense-Data Storage** **Kyomin Sohn,** *Samsung, Yongin, Korea*
12:00 PM	Lunch
1:20 PM	**Computation-in-Memory Circuit Design for Computing-Intensive and Storage-Intensive AI Applications** **Xin Si,** *Southeast University, Nanjing, China*
2:10 PM	**Reinventing Memory and Network Architecture for Large-Scale Energy-Efficient Low-Latency Generative AI** **Igor Arsovski,** *Groq, Williston, VT*
3:00 PM	Break
3:15 PM	**Optimizing Communication Between Chiplets for Future System-in-Packages** **Kemal Aygün,** *Intel, Chandler, AZ*
4:05 PM	**Complex Systems, Complex Threats: Security Strategies for Heterogeneous System Designs** **Todd M. Austin,** *University of Michigan, Ann Arbor, MI*
4:55 PM	Closing Remarks

FORUM 4

Highlights of Data-Converter R&D in the Past 5 Years: A Comprehensive Overview

Organizer:
Hajime Shibata, *Analog Devices, Toronto, Canada*
Lucien Breems, *NXP Semiconductors, Eindhoven, The Netherlands*

Co-Organizers:
Pieter Harpe, *Eindhoven University of Technology, Eindhoven, The Netherlands*
Il-Min Yi, *Gwangju Institute of Science and Technology, Gwangju, Korea*
Shiyu Su, *University of Waterloo, Waterloo, Canada*

Champions:
Kostas Doris, *NXP Semiconductors, Eindhoven, The Netherlands*
Matteo Bassi, *Infineon Technologies, Villach, Austria*

Moderator:
Matt Straayer, *Infineon Technologies, Andover, MA*

Every year at ISSCC, innovations are introduced, some of which become the norm, such as the asynchronous SAR ADC. It is easy to get left behind by these disruptive changes, even if you are an expert in a particular field. The purpose of this forum is to provide data converter experts with a comprehensive overview of the highlights (and lowlights!) of converter R&D over the past five years.

The forum will begin with a description of conventional data converter design techniques in various application and core technology areas. It will then cover disruptive technologies, new norms, and emerging trends in these areas. The goal is to provide new insights for experts in adjacent R&D areas to enjoy the beauty of cutting-edge innovations. It also aims to promote interdisciplinary understanding and foster yet another disruptive idea that will become a new norm in the next 5 years.

Thursday, February 20th, 8:00 AM

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Hajime Shibata,** *Analog Devices, Toronto, Canada*
8:25 AM	**AD Converter Figures of Merit: From a Meaningful Metric to a Design Disaster** **Bram Nauta,** *University of Twente, Enschede, The Netherlands*
9:10 AM	**High-Speed ADCs for 100Gb/s+ Wireline Transceivers** **Heng Zhang,** *Broadcom, Irvine, CA*
9:55 AM	Break
10:10 AM	**Developments and Challenges in High-Speed Continuous-Time ADCs for Wideband Wireless Communications** **Sharvil Patil,** *Analog Devices, Toronto, Canada*
10:55 AM	**High-Speed DAC Architectures and Techniques Towards High Dynamic Range, Bandwidth and Output Power** **Mike Shuo-Wei Chen,** *University of Southern California, Los Angeles, CA*
11:40 AM	**High-Performance Noise-Shaping ADCs** **Muhammed Bolatkale,** *NXP Semiconductors, Eindhoven, The Netherlands*
12:25 PM	Lunch
1:40 PM	**Highlights of Power-Efficient ADCs** **Youngcheol Chae,** *Yonsei University, Seoul, Korea*
2:25 PM	**Extending ADC Performance Through TDC-Assisted Quantization in Multiple Dimensions** **Minglei Zhang,** *University of Macau, Macau, China*
3:10 PM	Break
3:25 PM	**High-Performance Discrete-Time Amplifiers Utilizing Time-Varying Settling Processes** **Linxiao Shen,** *Peking University, Beijing, China*
4:10 PM	**Panel Discussions: Data Converter R&D for the Next 5 Years** **Moderator: Matt Straayer,** *Infineon Technologies, Andover, MA*
4:55 PM	Closing Remarks

Seeing the Future: Advances in Image and Vision Sensing

Organizers:
Andreas Suess, *Google, Mountain View, CA*
Min-Woong Seo, *Samsung Electronics Semiconductor R&D Center (SRDC), Hwaseong, Korea*

Co-Organizers:
Augusto Ximenes, *CogniSea, Seattle, WA*
Al Molnar, *Cornell University, Ithaca, NY*

Champions:
Makoto Ikeda, *University of Tokyo, Tokyo, Japan*
Bruce Rae, *STMicroelectronics, Edinburgh, United Kingdom*

Image sensors are the eyes of modern technology, enabling both humans and machines to perceive and interpret the world. While they are well-known in smartphones and cameras, their role in transformative applications such as autonomous vehicles, IoT devices, and AR/VR is rapidly growing. Advances like deep-trench isolation, 3D integration, and pixel-level innovations have driven the development of 2-layer pixels, miniaturized global shutters, time-of-flight sensing, and event-based detection. Stacked architectures, in particular, enable intelligent on-chip processing, making edge computing possible while reducing the device footprints for AR/VR, medical technology, and more. Metamaterials and computational cameras are further pushing boundaries by merging advanced optics with sophisticated algorithms, achieving higher image quality, enhanced depth perception, and entirely new imaging capabilities.

This forum provides engineers with insight into the latest breakthroughs in image sensor technology, edge computing, metaphotonics, and computational imaging—offering an inspiring platform to explore innovations that will shape the future of sensing and drive the next generation of technological advancements.

Thursday, February 20th, 8:00 AM

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Andreas Suess,** *Google, Mountain View, CA*
8:25 AM	**Innovative Image Sensors Technologies Expanding Applications and Market Frontiers** **Florian Domengie,** *Yole Group, Villeurbanne, France*
9:10 AM	**Dispersion-Engineered Metasurface Integration for Overcoming Pixel Shrink Limitations in CMOS Image Sensors** **Sookyoung Roh,** *Samsung Advanced Institute of Technology, Suwon, Korea*
9:55 AM	Break
10:10 AM	**Advances in Automotive CMOS Image Sensors** **Boyd A. Fowler,** *OMNIVISION, Santa Clara, CA*
10:55 AM	**Neuromorphic Imaging Sensor: How It Works and Its Applications** **Hyunsurk Eric Ryu,** *Seoul National University, Seoul, Korea*
11:40 AM	**Innovation Trends in Depth Sensing and Imaging: Enabling Technologies and Core Building Blocks** **David Stoppa,** *Sony Europe, Trento, Italy*
12:25 PM	Lunch
1:40 PM	**Photonics Enhanced Imaging for Omics and Medical Imaging** **Pol Van Dorpe,** *imec / Katholic University Leuven, Leuven, Belgium*
2:25 PM	**AI Sensors for Wearable Devices** **Chiao Liu,** *META, Redmond, WA*
3:10 PM	Break
3:25 PM	**From NIR to SWIR CMOS Image Sensors: Technology Challenges and state-of-the-art.** **Dominique Golanski,** *STMicroelectronics, Crolles, France*
4:10 PM	**Cameras As Nanophotonic Optical Computers** **Felix Heide,** *Princeton University, Princeton, NJ*
4:55 PM	Closing Remarks

Evolution of the Software-Defined Vehicle: Navigating Smart Cockpits and In-Car Hardware

Organizers:
Kazuki Fukuoka, *Renesas Electronics, Tokyo, Japan*
Eric Jia-Wei Fang, *Mediatek, Hsinchu, Taiwan*

Co-Organizers:
Sugako Otani, *Renesas Electronics, Tokyo, Japan*
Mina Shahmohammadi, *NXP Semiconductors, Delft, The Netherlands*
Hao Gao, *Southeast University, Nanjing, China*
Carlos Tokunaga, *Intel, Hillsboro, OR*

Champions:
Makoto Nagata, *Kobe University, Kobe, Japan*
Arun Natarajan, *Oregon State University, Corvallis, OR*

The automotive smart cockpit stands at the forefront of Software Defined Vehicles (SDV), intertwining sophistication with user-centric hardware innovations. By integrating advanced human-machine interfaces, 5G connectivity, and artificial intelligence, it profoundly elevates safety, customization, security, and entertainment through Over The Air (OTA) system. This integration not only caters to the escalating demands of modern consumers but is also instrumental in defining the trajectory of future mobility. As vehicles evolve into more autonomous entities, the smart cockpit becomes the critical nexus for enhanced user engagement, driving comfort, and overall vehicle intelligence. Consequently, it steers new Electrical/Electronic (E/E) architectures and state-of-the-art automotive grade LSIs. In this forum, experts will explain benefits and challenges in SDV of smart cockpits from each hardware component's point of view.

Thursday, February 20th, 8:00 AM

Agenda

Time	Topic
8:00 AM	Breakfast
8:15 AM	**Introduction** **Kazuki Fukuoka,** *Renesas Electronics, Tokyo, Japan*
8:25 AM	**Overview of Electrical and Electronic Architecture for Software Defined Vehicles** **Marius Rotaru,** *NXP Semiconductors, Munich, Germany*
9:15 AM	**Automotive 5G Technologies and RF/Baseband Chipsets for High Speed and Large Capacity Communication** **Feng Lu,** *Mediatek, Saratoga, CA*
10:05 AM	Break
10:20 AM	**Challenges in Automotive SoCs for Enabling Software-Defined Vehicles** **Yasuhisa Shimazaki,** *Renesas, Tokyo, Japan*
11:10 AM	**Understanding Over-The-Air Firmware Updates for Microcontrollers with Embedded Non-Volatile Memory** **Nicolas Grossier,** *STMicroelectronics, Agrate, Italy*
12:00 PM	Lunch
1:20 PM	**Radar Systems-on-Chip with Integrated Front-End, Processing, and Functional Safety for Automotive Applications** **Karthik Subburaj,** *Texas Instruments, Bangalore, India*
2:10 PM	**Privacy and Security Research Challenges for an Automotive Supplier** **Shalabh Jain,** *Bosch, Pittsburgh, PA*
3:00 PM	Break
3:15 PM	**Functional-Safe and Cybersecure Computing in Automotive Sensor Fusion Domains** **Udo Dannebaum,** *Infineon, Neubiberg, Germany*
4:05 PM	**Rethinking Autonomous Vehicle Development with AV Foundation Models** **Marco Pavone,** *Stanford and Nvidia, Stanford, CA*
4:55 PM	Closing Remarks

Advances in Wireless and RF Transceiver Circuits

Agenda

Time:	Topic:
8:00 AM	Breakfast
8:25 AM	Introduction by Chair, ***Daniel Friedman*** *IBM Thomas J. Watson Research Center, Yorktown Heights, NY*
8:30 AM	**Evolution of CMOS Radio Architectures** ***Behzad Razavi,*** *UCLA, Los Angeles, CA*
10:00 AM	Break
10:30 AM	**Multi-Antenna Radio Systems: MIMO and Phased Arrays** ***Arun Natarajan,*** *Oregon State University, Corvallis, OR*
12:15 PM	Lunch
1:20 PM	**Mixer-First and N-Path Architectures, Applications, and Research Directions** **Bram Nauta,** *University of Twente, Enschede, The Netherlands*
2:50 PM	Break
3:20 PM	**Transmitters: Power Amplifiers and Digitally Assisted RF** ***Morteza Alavi,*** *TU Delft, Delft, The Netherlands*
4:50 PM	Conclusion

Introduction

The interconnectedness of our world is enabled in no small part by advances in design for RF communications – the application of CMOS to radiofrequency design problems has revolutionized all aspects of wireless communication. This progress, driven by the phenomenal growth in demand for expanded communication capabilities, has been enabled by innovation in circuits and systems, resulting in the exceptionally capable radio systems in use today. Looking forward, emerging techniques for multi-antenna systems, receivers, and transmitters promise further extension of the abilities of such systems. In this short course, we start with a discussion of the evolution of CMOS radio architectures, including an introduction to the critical design considerations associated with modern RF systems. In the second lecture, we consider multi-antenna radio systems, including approaches for MIMO and phased array designs. In the third lecture, we consider receiver elements, focusing on mixer-first and N-path architectures, applications, and research directions. In the final talk, we consider transmitter elements, focusing on power amplifiers and emerging digitally assisted transmitter architectures.

8:30 AM

SC1: Evolution of CMOS Radio Architectures

Behzad Razavi, *UCLA, Los Angeles, CA*

The past three decades have witnessed tremendous advances in radios, with performance, cost, and power consumption driving both circuit design and architecture design. CMOS technology has afforded increasing sophistication in transceivers and led to effective methods of dealing with nonidealities.

CMOS radios continue to evolve so as to satisfy the demands of new applications. Below 7 GHz, cellular and WiFi standards have been pushing the performance to support increasingly higher data rates while consuming less power. Such endeavors require novel architectures that also lend themselves to efficient circuit design. In addition, new radios have emerged around 30 GHz for 5G, around 60 GHz for WiGig, around 140 GHz for 6G, and around 300 GHz for sub-terahertz communications. Each of these frequency bands presents interesting and unique challenges, but a unifying principle among them is the need for beamforming.

This presentation deals with past and recent developments in CMOS radio design for this broad range of applications. We examine the shortcomings of standard direct-conversion architectures and draw concepts from the state of the art to improve their performance. We also contend that heterodyne reception may outperform direct conversion in some cases and study "LO-friendly" architectures.

Behzad Razavi is Professor of Electrical Engineering at UCLA, where he conducts research on analog and RF integrated circuits. Prof. Razavi has served as an IEEE Distinguished Lecturer and published more than 200 papers and eight books. He has received nine IEEE best paper awards and six teaching and education awards, and his books have been published in seven languages. He received the IEEE Pederson Award in Solid-State Circuits and was recognized as a top author in the 50-year and 75-year histories of the IEEE International Solid-State Circuits Conference. He is a member of the US National Academy of Engineering and a fellow of the US National Academy of Inventors.

10:30 AM

SC2: Multi-Antenna Radio Systems: MIMO and Phased Arrays

Arun Natarajan, *Oregon State University, Corvallis, OR*

The increasing demand for wireless network capacity, constrained by the available spectrum, has motivated the development of phased-array and MIMO transceivers at RF and mm-wave frequencies. This lecture will explore architectures and design principles for integrated RF/mm-wave phased arrays and MIMO arrays. The lecture will also provide an overview of research in this field driving the next generation of wireless communication systems.

Arun Natarajan received a B.Tech. degree in Electrical Engineering from IIT Chennai in 2001, and Ph.D. in Electrical Engineering from Caltech in 2007. From 2007 to 2012, he was a Research Staff Member with IBM T. J. Watson Research Center. In 2012, he joined Oregon State University where he is currently a Professor in the School of Electrical Engineering and Computer Science. His research focuses on RF and mm-wave integrated circuits and systems for wireless communication and imaging. He was also a part of the leadership team of Mixcomm Inc., a venture-funded startup focused on mm-wave phased-array ICs and systems for 5G and Satcom. Mixcomm Inc. was acquired by Sivers Semiconductors in 2022.

1:20 PM

SC3: Mixer-First and N-Path Architectures, Applications, and Research Directions

Bram Nauta, *University of Twente, Enschede, The Netherlands*

In this lecture, mixer-first architectures are introduced. These architectures do not use a low-noise amplifier but instead employ a low-loss passive mixer. These passive mixers exhibit very good linearity and also offer the option of narrow-band RF filtering right at the input of the mixer. The RF filtering is achieved by exploiting the mixer in a so-called N-path filter, which is a filtering technique from forgotten times. This ability to filter at RF makes the mixer-first receiver a good candidate for application where interference is a challenge.

New ideas, such as higher-order filtering and passive voltage gain through capacitor stacking, will also be presented in this lecture. Additionally, an outlook on fully passive receivers is also given as a possible future direction.

Bram Nauta was born in Hengelo, The Netherlands. In 1987, he received the M.Sc. degree and the Ph.D. degree, both from the University of Twente, Enschede, The Netherlands. In 1991, he joined the Mixed-Signal Circuits and Systems Department of Philips Research, Eindhoven, the Netherlands. In 1998, he returned to the University of Twente as a full professor, heading the IC Design group. He was nominated as Distinguished Professor in 2014.

He served as the Editor-in-Chief (2007-2010) of the IEEE Journal of Solid-State Circuits (JSSC) and was the 2013 program chair of the International Solid-State Circuits Conference (ISSCC). He served as the President of the IEEE Solid-State Circuits Society (2018-2019 term).

3:20 PM

SC4: Transmitters: Power Amplifiers and Digitally Assisted RF

Morteza Alavi, *TU Delft, Delft, The Netherlands*

The transmitter (TX) is a critical building block in wireless communication systems. This short course first overviews two main analog-intensive TX architectures, their sub-blocks, and TX system requirements. The talk then introduces efficiency-enhanced power amplifiers (PAs), (double) quadrature modulators, and new emerging digital-intensive TXs. It discusses their strengths, potential, and challenges while presenting a few modern TX architectures and PAs.

Morteza S. Alavi received his Ph.D. in Electrical Engineering from TU-Delft in 2014. In September 2016, he joined the Electronic Circuits and Architectures (ELCA) research group at TU-Delft, where he is currently a tenured Assistant Professor. His main research interest is in designing RFICs for wireless, wireline, and cellular communication systems.

ISSCC 2025 EXECUTIVE COMMITTEE

CONFERENCE CHAIR
Edith Beigné
Meta, Menlo Park, CA

PAST CONFERENCE CHAIR AND ADCOM REP
Eugenio Cantatore
Eindhoven University of Technology, Eindhoven, The Netherlands

STEERING COMMITTEE CHAIR
Anantha Chandrakasan
Massachusetts Institute of Technology, Cambridge, MA

EXECUTIVE COMMITTEE SECRETARY
Makoto Nagata
Kobe University, Kobe, Japan

PROGRAM CHAIR
Thomas Burd
Advanced Micro Devices, Santa Clara, CA

PROGRAM VICE-CHAIR
Keith Bowman
Qualcomm, Raleigh, NC

PAST PROGRAM CHAIR
Frank O'Mahony
Apple, Beaverton, OR

ITPC FAR EAST REGIONAL CHAIR
Jaehyouk Choi
Seoul National University, Seoul, Korea

ITPC FAR EAST REGIONAL VICE-CHAIR
Wei-Zen Chen
National Yang Ming Chiao Tung University, Hsinchu, Taiwan

ITPC EUROPEAN REGIONAL CHAIR
Matteo Bassi
Infineon Technologies AG, Villach, Austria

ITPC EUROPEAN REGIONAL VICE-CHAIR
Jens Anders
University of Stuttgart, Stuttgart, Germany

ITPC NORTH AMERICA REGIONAL CHAIR
Jeff Walling
Virginia Tech, Blacksburg, VA

ITPC NORTH AMERICA REGIONAL VICE CHAIR
Danielle Grifith
Texas Instruments, Dallas, TX

DEMO SESSION CHAIR
Patrick Mercier
University of California, San Diego, La Jolla, CA

SRP CHAIR
Jerald Yoo
Seoul National University, Seoul, Korea

ADCOM REPRESENTATIVE
Jan van der Spiegel
University of Pennsylvania, Philadelphia, PA

DIRECTOR OF PUBLICATIONS, PRESS-RELATIONS LIAISON
Laura Fujino
University of Toronto, Toronto, Canada

PRESS COORDINATOR
Shahriar Mirabbasi
University of British Columbia, Vancouver, Canada

EDUCATIONAL EVENTS CHAIR
Ali Sheikholeslami
University of Toronto, Toronto, Canada

DIRECTOR OF OPERATIONS
Melissa Widerkehr
Widerkehr and Associates, Lewes, DE

DIRECTOR OF FINANCE
John Weinmann
Rochester, NY

WEB SITE AND A/V CHAIR
Trudy Stetzler
Halliburton, Houston, TX

SOCIAL MEDIA CHAIR
Vito Giannini
Uhnder, Austin, TX

WIC REPRESENTATIVE
Farhana Sheikh
Altera, Portland, OR

INDUSTRY CHAIR
Alicia Klinefelter
NVidia, Durham, NC

INDUSTRY CHAIR
Vivek De
Intel, Hillsboro, OR

EXHIBITION CHAIR
Eric Karl
Intel

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

Technical Editors & Multi-Media Coordinator

Jason H. Anderson, *University of Toronto, Toronto, Canada*
Leonid Belostotski, *The University of Calgary, Calgary, Canada*
Dustin Dunwell, *Alphawave IP, Toronto, Canada*
Vincent Gaudet, *University of Waterloo, Waterloo, Canada*
Glenn Gulak, *University of Toronto, Toronto, Canada*
James W. Haslett, *The University of Calgary, Calgary, Canada*
Shahriar Mirabbasi, *University of British Columbia, Vancouver, Canada*
Samantha Murray, *StarIC, Toronto, Canada*

MULTI-MEDIA COORDINATOR AND DIGEST EDITOR

David Halupka, *StarIC, Toronto, Canada*

Analog Subcommittee

Chair: Viola Schaffer, *Texas Instruments, Freising, Germany*

Ippei Akita, *AIST, Tsukuba, Japan*
Jens Anders, *University of Stuttgart, Stuttgart, Germany*
Chinwuba Ezekwe, *Robert Bosch, Sunnyvale, CA*
Qinwen Fan, *Delft University of Technology, Delft, The Netherlands*
Danielle Grifith, *Texas Instruments, Dallas, TX*
Drew Hall, *University of California, San Diego, La Jolla, CA*
Chuan-Hung Hsiao, *MediaTek, Hsinchu City, Taiwan*
Minkyu Je, *KAIST, Daejeon, Korea*
Qiang Li, *University of Electronic Science and Technology of China, Chengdu, China*
Giulio Ricotti, *STMicroelectronics, Cornaredo, Italy*
Caspar van Vroonhoven, *Analog Devices, Ismaning,Germany*
Jiawei Xu. *Fudan University, Shanghai, China*

Data Converters Subcommittee

Chair: Jan Westra, *Broadcom, Bunnik, The Netherlands*

Lucien J. Breems, *NXP Semiconductors, Eindhoven, The Netherlands*
Vanessa Chen, *Carnegie Mellon University, Pittsburgh, PA*
Pieter Harpe, *Eindhoven University of Technology, Eindhoven, The Netherlands*
Wan Kim, *Samsung Electronics, Hwaseong, Korea*
Ying-Zu Lin*, *Mediatek, Hsinchu, Taiwan*
Nima Maghari, *University of Florida, Gainesville, FL*
Shahrzad Naraghi, *Legato Logic, San Jose, CA*
Shanthi Pavan, *IIT Madras, Chennai, India*
Seung-Tak Ryu, *KAIST, Daejeon, Korea*
Hajime Shibata, *Analog Devices, Toronto, Canada*
Shiyu Su, *University of Waterloo, Waterloo, Canada*
Xiyuan Tang, *Peking University, Beijing, China*
Amy Whitcombe, *Intel, Santa Clara, CA*
Il-Min Yi, *Gwangju Institute of Science and Technology, Gwangju, Korea*
**1981 to 2024*

Digital Architectures & Systems (DAS) Subcommittee

Chair: Rahul Rao, *IBM India, Bangalore, India*

Mark A. Anders, *Intel, Hillsboro, OR*
Shidhartha Das, *Advanced Micro Devices, Cambridge, United Kingdom*
Jie Gu, *Northwestern University, Evanston, IL*
Ji-Hoon Kim, *Ewha Womans University, Seoul, Korea*
Hugh Mair, *MediaTek, Austin, TX*
Bert Moons, *Axelera AI, Leuven, Belgium*
Sugako Otani, *Renesas Electronics, Tokyo, Japan*
Nathaniel Pinckney, *Nvidia, Austin, TX*
Priyanka Raina, *Stanford University, Stanford, CA*
Soojung Ryu, *Seoul National University, Seoul, Korea*
Paul Whatmough, *Qualcomm, Boston, MA*
Chia-Hsiang Yang, *National Taiwan University, Taipei, Taiwan*
Jun Zhou, *Univeristy of Electronic Science and Technology of China, Chengdu, China*

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

Digital Circuits (DCT) Subcommittee

Chair: Huichu Liu, *Meta, Sunnyvale, CA*

Benton Calhoun, *University of Virginia, Charlottesville, VA*
Sylvain Clerc, *STMicroelectronics, Crolles, France*
Eric Jia-Wei Fang, *Mediatek, Hsinchu, Taiwan*
Kazuki Fukuoka, *Renesas Electronics, Tokyo, Japan*
Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*
Jun-Seok Park, *S.LSI, Samsung Electronics, Hwaseong, Korea*
Arijit Raychowdhury, *Georgia Institute of Technology, Atlanta, GA*
Visvesh Sathe, *Georgia Institute of Technology, Atlanta, GA*
Jae-sun Seo, *Cornell Tech, New York, NY*
Mahmut Ersin Sinangil, *Nvidia, Santa Clara, CA*
Yvain Thonnart, *CEA-List, Grenoble, France*
Carlos Tokunaga, *Intel, Hillsboro, OR*
Kaushik Vaidyanathan, *OpenAI, San Francisco, CA*
Masanao Yamaoka, *Hitachi, Tokyo, Japan*
Heein Yoon, *Ulsan National Institute of Science and Technology, Ulsan, Korea*

IMD Subcommittee

Chair: Rikky Muller, *University of California, Berkeley, Berkeley, CA*

Jun-Chau Chien, *University of California, Berkeley, Berkeley, CA*
Azita Emami, *California Institute of Technology, Pasadena, CA*
Leonardo Gasparini, *Fondazione Bruno Kessler, Trento, Italy*
Sohmyung Ha, *New York University;*
New York University Abu Dhabi, Abu Dhabi, UAE
Mutsumi Hamaguchi, *Sharp Corporation, Tenri, Japan*
Taekwang Jang, *ETH Zurich, Zurich, Switzerland*
Mehdi Kiani, *The Pennsylvania State University, University Park, PA*
Hyung-Min Lee, *Korea University, Seoul, Korea*
Junghyup Lee, *DGIST, Daegu, Korea*
Carolina Mora-Lopez, *Imec, Leuven, Belgium*
Masaki Sakakibara, *Sony Semiconductor Solutions Corporation, Atsugi, Japan*
Min-Woong Seo, *Samsung Electronics, Hwaseong, Korea*
Sanshiro Shishido, *Panasonic Holdings Corporation, Kadoma, Japan*
Mahsa Shoaran, *EPFL, Geneva, Switzerland*
Andreas Suess, *Google, Mountain View, CA*
Kea-Tiong (Samuel) Tang, *National Tsing Hua University, Hsinchu, Taiwan*
Augusto Ximenes, *CogniSea, Inc., Seattle, WA*
Bo Zhao, *Zhejiang University, Hangzhou, China*

Memory Subcommittee

Chair: Meng-Fan Chang, *National Tsing Hua University, Hsinchu, Taiwan*

Juang-Ying Chueh, *Etron Technology, Taipei, Taiwan*
Chunmeng Dou, *Chinese Academy of Sciences, Beijing, China*
Zheng Guo, *Intel, Portland, OR*
Thomas Hein, *Micron, Munich, Germany*
Hua-Ling (Cynthia) Hsu, *Western Digital, Fremont, CA*
Takashi Ito, *Renesas, Tokyo, Japan*
Dongkyun Kim, *SK hynix, Icheon, Korea*
Hye-Ran Kim, *Samsung Electronics, Anyang, Korea*
Saekyu Lee, *EnCharge AI, Denver, CO*
Seung-Jae Lee, *Samsung Electronics, Hwaseong, Korea*
Xueqing Li, *Tsinghua University, Beijing, China*
Violante Moschiano, *OpenChip Technologies, Barcelona, Spain*
Hidehiro Shiga, *KIOXIA, Yokohama, Japan*
Eric Wang, *TSMC, Hsinchu, Taiwan*
John Wuu, *Advanced Micro Devices, Fort Collins, CO*
Jun Yang, *Southeast University, Nanjing, China*

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

Power Management Subcommittee

Chair: Bernhard Wicht, *University of Hannover, Hannover, Germany*

Interim Vice-Chair: Saurav Bandyopadhyay, *Texas Instruments, Dallas, TX*

Sally Amin, *Apple, Cupertino, CA*
Patrik Arno, *STMicroelectronics, Grenoble, France*
Lin Cheng, *University of Science and Technology of China, Hefei, China*
Chen-Yen Ho, *MediaTek, Hsinchu, Taiwan*
Sung-Wan Hong, *Sogang University, Seoul, Korea*
Mo Huang, *University of Macau, Taipa, Macao, China*
Rinkle Jain, *Nvidia, Santa Clara, CA*
Shusuke Kawai, *Toshiba, Kawasaki, Japan*
Xugang Ke, *Zhejiang University, Hangzhou, China*
Dongsu Kim, *Samsung Electronics, Hwaseong, Korea*
Hyun-Sik Kim, *KAIST, Daejeon, Korea*
Hanh-Phuc Le, *University of California, San Diego, La Jolla, CA*
Xun Liu, *The Chinese University of Hong Kong, Shenzhen, China*
Kousuke Miyaji, *Shinshu University, Nagano, Japan*
John Pigott, *NXP, Chandler, AZ*
Gael Pillonnet, *CEA-Leti, Grenoble, France*
Frank Prämaßing, *Infineon Technologies Austria AG, Villach, Austria*
Joseph (Joey) Sankman, *Analog Devices, Fort Collins, CO*
Xin Zhang, *IBM T. J. Watson Research Center, Yorktown Heights, NY*

RF Subcommittee

Chair: Brian Ginsburg, *Texas Instruments, Dallas, TX*

Interim Vice-Chair: Masoud Babaie, *Delft University of Technology, Delft, The Netherlands*

Sudipto Chakraborty, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Dmytro Cherniak, *Infineon Technologies, Villach, Austria*
Jaehyouk Choi, *Seoul National University, Seoul, Korea*
Debabani Choudhury, *Intel, CA*
Wei Deng, *Tsinghua University, Beijing, China*
Jeremy Dunworth, *Qualcomm Technologies Inc., San Diego, CA*
Xiang Gao, *Zhejiang University, Hangzhou, China*
Hiroshi Hamada, *NTT, Atsugi, Japan*
Ruonan Han, *Massachusetts Institute of Technology, Cambridge, MA*
Mona Hella*, *Rensselaer Polytechnic Institute, Troy, NY*
Yu-Li Hsueh, *Mediatek, Hsinchu, Taiwan*
Danilo Manstretta, *University of Pavia, Pavia, Italy*
Omeed Momeni, *University of California, Davis, Davis, CA*
Mina Shahmohammadi, *NXP Semiconductors, Delft, The Netherlands*
Henrik Sjöland, *Lund University, Ericsson Research, Lund, Sweden*
Jeff Walling, *Virginia Tech., Blacksburg, VA*
Hongtao Xu, *Fudan University, Shanghai, China*
Jun Yin, *University of Macau, Taipa, Macau, China*

Security Subcommittee

Chair: Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*

Utsav Banerjee, *Indian Institute of Science, Bengaluru, India*
Chiraag Juvekar, *Apple, San Carlos, CA*
Yong Ki Lee, *Samsung Electronics, Suwon, Korea*
Leibo Liu, *Tsinghua University, Beijing, China*
Sanu Mathew, *Intel, Hillsboro, OR*
Thomas Poeppelmann, *Infineon Technologies, Neubiberg, Germany*
Shreyas Sen, *Purdue University, West Lafayette, IN*
Takeshi Sugawara, *The University of Electro-Communications, Tokyo, Japan*
Rabia Tugce Yazicigil, *Boston University, Boston, MA*

**1971 to 2025*

INTERNATIONAL TECHNICAL PROGRAM COMMITTEE

Technology Directions Subcommittee

Chair: Ali Hajimiri, *Caltech, Pasadena, CA*

Firooz Aflatouni, *University of Pennsylvania, Philadelphia, PA*
Joseph Bardin, *Google & UMass Amherst, Goleta, CA*
Denis Daly, *Apple, Waltham, MA*
Giorgio Ferrari, *Politecnico di Milano, Milano, Italy*
Shawn Shuo-Hung Hsu, *National Tsing Hua University, Hsinchu, Taiwan*
Kyeongha Kwon, *KAIST, Daejeon, Korea*
Noriyuki Miura, *Osaka University, Osaka, Japan*
Alyosha Molnar, *Cornell University, Ithaca, NY*
Daniel H. Morris, *OpenAI, San Francisco, CA*
Jacques "Chris" Rudell, *University of Washington, Seattle, WA*
Fabio Sebastiano, *Delft University of Technology, Delft, The Netherlands*
Kaushik Sengupta, *Princeton University, Princeton, NJ*
Guy Torfs, *Ghent University, Gent, Belgium*
Kaiyuan Yang, *Rice University, Houston, TX*
Milin Zhang, *Tsinghua University, Beijing, China*

Wireless Subcommittee

Chair: Chih-Ming Hung, *MediaTek, Taipei, Taiwan*

Matteo Bassi, *Infineon Technologies AG, Villach, Austria*
Wu-Hsin Chen, *Qualcomm, San Diego, CA*
Hao Gao, *Southeast University, Nanjing, China*
Giuseppe Gramegna, *imec, Leuven, Belgium*
Jane Gu, *Georgia Institute of Technology, Atlanta, GA*
Kuo-Ken Huang, *Everactive, San Jose, CA*
Renzhi Liu, *Apple, Beaverton, OR*
Byung-Wook Min, *Yonsei University, Seoul, Korea*
Jan Prummel, *Renesas Design Netherlands B.V., 's-Hertogenbosch, The Netherlands*
Raja Pullela, *Maxlinear, Irvine, CA*
Negar Reiskarimian, *Massachusetts Institute of Technology, Cambridge, MA*
Shahriar Shahramian, *Nokia – Bell Labs, New Providence, NJ*
Ho-Jin Song, *Pohang University of Science and Technology, Pohang, Korea*
Alberto Valdes-Garcia, *IBM Research, Yorktown Heights, NY*
Yun Yin, *Fudan University, Shanghai, China*
Yuanjin Zheng, *Nanyang Technological University, Singapore, Singapore*
Alireza Zolfaghari, *Broadcom, Irvine, CA*

Wireline Subcommittee

Chair: Thomas Toifl, *Cisco Systems, Thalwil, Switzerland*

Tamer Ali, *Mediatek, Irvine, CA*
Wei-Zen Chen, *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*
Zeynep Toprak Deniz, *IBM Research, Yorktown Heights, NY*
Masum Hossain, *Carleton University, Ottawa, Canada*
Kenny Hsieh, *TSMC, Hsinchu, Taiwan*
Jay Im, *AMD, San Jose, CA*
Mozhgan Mansuri, *Intel, Hillsboro, OR*
Didem Turker Melek, *Cadence Design Systems, San Jose, CA*
Peter Ossieur, *Imec, University of Ghent, Ghent, Belgium*
Ben Rhew, *Samsung, Hwaseong, Korea*

EUROPEAN REGIONAL SUBCOMMITTEE

ITPC EUROPEAN REGIONAL CHAIR
Matteo Bassi
Infineon Technologies AG, Villach, Austria

ITPC EUROPEAN REGIONAL VICE CHAIR
Jens Anders, *University of Stuttgart, Stuttgart, Germany*

ITPC EUROPEAN REGIONAL SECRETARY
Qinwen Fan, *Delft University of Technology, Delft, The Netherlands*

Patrik Arno, *STMicroelectronics, Grenoble, France*
Masoud Babaie, *Delft University of Technology, Delft, The Netherlands*
Lucien J. Breems, *NXP Semiconductors, Eindhoven, The Netherlands*
Dmytro Cherniak, *Infineon Technologies, Villach, Austria*
Sylvain Clerc, *STMicroelectronics, Crolles, France*
Shidhartha Das, *Advanced Micro Devices, Cambridge, United Kingdom*
Giorgio Ferrari, *Politecnico di Milano, Milano, Italy*
Leonardo Gasparini, *Fondazione Bruno Kessler, Povo, Italy*
Giuseppe Gramegna, *imec, Leuven, Belgium*
Sohmyung Ha, *New York University; New York University Abu Dhabi, Abu Dhabi, UAE*
Pieter Harpe, *Eindhoven University of Technology, Eindhoven, The Netherlands*
Thomas Hein, *Micron, Munich, Germany*
Taekwang Jang, *ETH Zurich, Zurich, Switzerland*
Danilo Manstretta, *University of Pavia, Pavia, Italy*
Bert Moons, *Axelera AI, Leuven, Belgium*
Carolina Mora-Lopez, *Imec, Leuven, Belgium*
Violante Moschiano, *OpenChip Technologies, Barcelona, Spain*
Peter Ossieur, *Imec, University of Ghent, Ghent, Belgium*
Gael Pillonnet, *CEA-Leti, Grenoble, France*
Thomas Poeppelmann, *Infineon Technologies, Neubiberg, Germany*
Frank Prämaßing, *Infineon Technologies Austria AG, Villach, Austria*
Jan Prummel, *Renesas Design Netherlands B.V., 's-Hertogenbosch, The Netherlands*
Giulio Ricotti, *STMicroelectronics, Cornaredo, Italy*
Viola Schaffer, *Texas Instruments, Freising, Germany*
Fabio Sebastiano, *Delft University of Technology, Delft, The Netherlands*
Mina Shahmohammadi, *NXP Semiconductors, The Netherlands*
Mahsa Shoaran, *EPFL, Geneva, Switzerland*
Henrik Sjöland, *Lund University, Ericsson Research, Lund, Sweden*
Yvain Thonnart, *CEA-List, Grenoble, France*
Thomas Toifl, *Cisco Systems, Thalwil, Switzerland*
Guy Torfs, *Ghent University, Gent, Belgium*
Caspar van Vroonhoven, *Analog Devices, Ismaning, Germany*
Ingrid Verbauwhede, *KU Leuven, Leuven, Belgium*
Jan Westra, *Broadcom, Bunnik, The Netherlands*
Bernhard Wicht, *University of Hannover, Hannover, Germany*

FAR EAST REGIONAL SUBCOMMITTEE

ITPC FAR EAST REGIONAL CHAIR
Jaehyouk Choi, *Seoul National University, Seoul, Korea*

ITPC FAR EAST REGIONAL VICE CHAIR
Wei-Zen Chen, *National Yang Ming Chiao Tung University, Hsinchu, Taiwan*

ITPC FAR EAST REGIONAL SECRETARY
Kousuke Miyaji, *Shinshu University, Nagano, Japan*

ITPC FAR-EAST REGIONAL ASSOCIATE SECRETARY
Jun Yin, *University of Macau, Taipa, Macau, China*

Ippei Akita, *AIST, Tsukuba, Japan*
Utsav Banerjee, *Indian Institute of Science, Bengaluru, India*
Meng-Fan Chang, *National Tsing Hua University, Hsinchu, Taiwan*
Lin Cheng, *University of Science and Technology of China, Hefei, China*
Juang-Ying Chueh, *Etron Technology, Taipei, Taiwan*
Wei Deng, *Tsinghua University School of Integrated Circuits, Beijing, China*
Chunmeng Dou, *Chinese Academy of Sciences, Beijing, China*
Eric Jia-Wei Fang, *Mediatek, Hsinchu, Taiwan*
Kazuki Fukuoka, *Renesas Electronics, Tokyo, Japan*
Hao Gao, *Southeast University, Nanjing, China*
Xiang Gao, *Zhejiang University, Hangzhou, China*
Hiroshi Hamada, *NTT, Atsugi, Japan*
Mutsumi Hamaguchi, *Sharp Corporation, Tenri, Japan*
Chen-Yen Ho, *MediaTek, Hsinchu, Taiwan*
Sung-Wan Hong, *Sogang University, Seoul, Korea*
Chuan-Hung Hsiao, *MediaTek, Hsinchu, Taiwan*
Kenny Hsieh, *TSMC, Hsinchu, Taiwan*
Ping-Hsuan Hsieh, *National Tsing Hua University, Hsinchu, Taiwan*
Shawn Shuo-Hung Hsu, *National Tsing Hua University, Hsinchu, Taiwan*
Yu-Li Hsueh, *Mediatek, Hsinchu, Taiwan*
Mo Huang, *University of Macau, Taipa, Macao, China*
Chih-Ming Hung, *MediaTek, Taipei, Taiwan*
Takashi Ito, *Renesas, Tokyo, Japan*
Minkyu Je, *KAIST, Daejeon, Korea*
Shusuke Kawai, *Toshiba, Kawasaki, Japan*
Xugang Ke, *Zhejiang University, Hangzhou, China*
Dongkyun Kim, *SK hynix, Icheon, Korea*
Dongsu Kim, *Samsung Electronics, Hwaseong, Korea*
Hye-Ran Kim, *Samsung Electronics, Anyang, Korea*
Hyun-Sik Kim, *KAIST, Daejeon, Korea*
Ji-Hoon Kim, *Ewha Womans University, Seoul, Korea*
Wan Kim, *Samsung Electronics, Hwaseong, Korea*
Kyeongha Kwon, *KAIST, Daejeon, Korea*
Hyung-Min Lee, *Korea University, Seoul, Korea*
Junghyup Lee, *DGIST, Daegu, Korea*
Seung-Jae Lee, *Samsung Electronics, Hwaseong, Korea*
Yong Ki Lee, *Samsung Electronics, Suwon, Korea*
Qiang Li, *University of Electronic Science and Technology of China, Chengdu, China*
Xueqing Li, *Tsinghua University, Beijing, China*
Ying-Zu Lin*, *Mediatek, Hsinchu, Taiwan*
Leibo Liu, *Tsinghua University, Beijing, China*
Xun Liu, *The Chinese University of Hong Kong, Shenzhen, China*
Byung-Wook Min, *Yonsei University, Seoul, Korea*
Noriyuki Miura, *Osaka University, Osaka, Japan*
Sugako Otani, *Renesas Electronics, Tokyo, Japan*

**1981 to 2024*

FAR EAST REGIONAL SUBCOMMITTEE

Jun-Seok Park, *S.LSI, Samsung Electronics, Hwaseong, Korea*
Shanthi Pavan, *IIT Madras, Chennai, India*
Rahul Rao, *IBM India, Bangalore, India*
Ben Rhew, *Samsung, Hwaseong, Korea*
Seung-Tak Ryu, *Seoul National University, Seoul, Korea*
Soojung Ryu, *Seoul National University, Seoul, Korea*
Masaki Sakakibara, *Sony Semiconductor Solutions Corporation, Atsugi, Japan*
Min-Woong Seo, *Samsung Electronics, Hwaseong, Korea*
Hidehiro Shiga, *KIOXIA, Yokohama, Japan*
Sanshiro Shishido, *Panasonic Holdings Corporation, Kadoma, Japan*
Ho-Jin Song, *Pohang University of Science and Technology, Pohang, Korea*
Takeshi Sugawara, *The University of Electro-Communications, Tokyo, Japan*
Kea-Tiong (Samuel) Tang, *National Tsing Hua University, Hsinchu, Taiwan*
Xiyuan Tang, *Peking University, Beijing, China*
Eric Wang, *TSMC, Hsinchu, Taiwan*
Hongtao Xu, *Fudan University, Shanghai, China*
Jiawei Xu, *Fudan University, Shanghai, China*
Masanao Yamaoka, *Hitachi, Tokyo, Japan*
Chia-Hsiang Yang, *National Taiwan University, Taipei, Taiwan*
Jun Yang, *Southeast University, Nanjing, China*
Il-Min Yi, *Gwangju Institute of Science and Technology, Gwangju, Korea*
Yun Yin, *Fudan University, Shanghai, China*
Heein Yoon, *Ulsan National Institute of Science and Technology, Ulsan, Korea*
Bo Zhao, *Zhejiang University, Hangzhou, China*
Milin Zhang, *Tsinghua University, Beijing, China*
Yuanjin Zheng, *Nanyang Technological University, Singapore, Singapore*
Jun Zhou, *Univeristy of Electronic Science and Technology of China, Chengdu, China*

NORTH AMERICA REGIONAL SUBCOMMITTEE

ITPC NORTH AMERICA REGIONAL CHAIR
Jeff Walling, *Virginia Tech., Blacksburg, VA*

ITPC NORTH AMERICA REGIONAL VICE CHAIR
Danielle Grifith, *Texas Instruments, Dallas, TX*

ITPC NORTH AMERICA REGIONAL SECRETARY
John Wuu, *Advanced Micro Devices, Fort Collins, CO*

Firooz Aflatouni, *University of Pennsylvania, Philadelphia, PA*
Tamer Ali, *Mediatek, Irvine, CA*
Sally Amin, *Apple, Cupertino, CA*
Mark A. Anders, *Intel, Hillsboro, OR*
Saurav Bandyopadhyay, *Texas Instruments, Dallas, TX*
Joseph Bardin, *Google & UMass Amherst, Goleta, CA*
Benton Calhoun, *University of Virginia, Charlottesville, VA*
Sudipto Chakraborty, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Vanessa Chen, *Carnegie Mellon University, Pittsburgh, PA*
Wu-Hsin Chen, *Qualcomm, San Diego, CA*
Jun-Chau Chien, *University of California, Berkeley, Berkeley CA*
Debabani Choudhury, *Intel, CA*
Denis Daly, *Apple, Waltham, MA*
Zeynep Toprak Deniz, *IBM Research, Yorktown Heights, NY*
Jeremy Dunworth, *Qualcomm Technologies Inc., San Diego, CA*
Azita Emami, *California Institute of Technology, Pasadena, CA*
Chinwuba Ezekwe, *Robert Bosch, Sunnyvale, CA*
Brian Ginsburg, *Texas Instruments, Dallas, TX*
Jane Gu, *Georgia Institute of Technology, Atlanta, GA*
Jie Gu, *Northwestern University, Evanston, IL*
Zheng Guo, *Intel, Portland, OR*
Ali Hajimiri, *Caltech, Pasadena, CA*
Drew Hall, *University of California, San Diego, La Jolla, CA*
Ruonan Han, *Massachusetts Institute of Technology, Cambridge, MA*
Mona Hella*, *Rensselaer Polytechnic Institute, Troy, NY*
Masum Hossain, *Carleton University, Ottawa, Canada*
Hua-Ling (Cynthia) Hsu, *Western Digital, Fremont, CA*
Kuo-Ken Huang, *Everactive, San Jose, CA*
Jay Im, *AMD, San Jose, CA*
Rinkle Jain, *Nvidia, Santa Clara, CA*
Chiraag Juvekar, *Apple, San Carlos, CA*
Mehdi Kiani, *The Pennsylvania State University, University Park, PA*
Hanh-Phuc Le, *University of California, San Diego, La Jolla, CA*
Saekyu Lee, *EnCharge AI, Denver, CO*
Huichu Liu, *Meta, Sunnyvale, CA*
Renzhi Liu, *Apple, Beaverton, OR*
Nima Maghari, *University of Florida, Gainesville, FL*
Hugh Mair, *MediaTek, Austin, TX*
Mozhgan Mansuri, *Intel, Hillsboro, OR*
Sanu Mathew, *Intel, Hillsboro, OR*
Didem Turker Melek, *Cadence Design Systems, San Jose, CA*
Alyosha Molnar, *Cornell University, Ithaca, NY*
Omeed Momeni, *University of California, Davis, Davis, CA*
Daniel H. Morris, *OpenAI, San Francisco, CA*
Rikky Muller, *University of California, Berkeley, Berkeley, CA*
Shahrzad Naraghi, *Legato Logic, San Jose, CA*
John Pigott, *NXP, Chandler, AZ*
Nathaniel Pinckney, *Nvidia, Austin, TX*
Raja Pullela, *Maxlinear, Irvine, CA*
Priyanka Raina, *Stanford University, Stanford, CA*

**1971 to 2025*

NORTH AMERICA REGIONAL SUBCOMMITTEE

Arijit Raychowdhury, *Georgia Institute of Technology, Atlanta, GA*
Negar Reiskarimian, *Massachusetts Institute of Technology, Cambridge, MA*
Jacques "Chris" Rudell, *University of Washington, Seattle, WA*
Joseph (Joey) Sankman, *Analog Devices, Fort Collins, CO*
Visvesh Sathe, *Georgia Institute of Technology, Atlanta, GA*
Jae-sun Seo, *Cornell Tech, New York, NY*
Shreyas Sen, *Purdue University, West Lafayette, IN*
Kaushik Sengupta, *Princeton University, Princeton, NJ*
Shahriar Shahramian, *Nokia – Bell Labs, New Providence, NJ*
Hajime Shibata, *Analog Devices, Toronto, Canada*
Mahmut Ersin Sinangil, *Nvidia, Santa Clara, CA*
Shiyu Su, *University of Waterloo, Waterloo, Canada*
Andreas Suess, *Google, Mountain View, CA*
Carlos Tokunaga, *Intel, Hillsboro, OR*
Kaushik Vaidyanathan, *OpenAI, San Francisco, CA*
Alberto Valdes-Garcia, *IBM Research, Yorktown Heights, NY*
Paul Whatmough, *Qualcomm, Boston, MA*
Amy Whitcombe, *Intel, Santa Clara, CA*
Augusto Ximenes, *CogniSea, Inc., Seattle, WA*
Kaiyuan Yang, *Rice University, Houston, TX*
Rabia Tugce Yazicigil, *Boston University, Boston, MA*
Xin Zhang, *IBM T. J. Watson Research Center, Yorktown Heights, NY*
Alireza Zolfaghari, *Broadcom, Irvine, CA*

HOW TO REGISTER FOR ISSCC

Online: This is the only way to register and will give you immediate email confirmation of your events. Go to the ISSCC website at www.isscc.org and select the link to the Registration website.

Payment Options: Immediate payment can be made online via credit card. **Registrations received without full payment will not be processed until payment is received at YesEvents.** Please read the instructions on the Registration website.

COVID 19 PROTOCOLS

The health and safety of our conference attendees is our top priority. The ISSCC 2025 conference Organizing Committee remains vigilant in monitoring the COVID-19 pandemic. The conference will follow CDC and State of California guidelines. ISSCC is planned as an in-person event but it also has an online offering. We look forward to you joining us in San Francisco, CA. If you don't feel comfortable participating in large gatherings, or if your organization has travel restrictions, we encourage you to join us online.

MASKS, VACCINATION, SANITIZERS

Masks help slow the spread of the virus. They help to protect the medically vulnerable and those unable to get vaccinated. In San Francisco there are no longer masking requirements for most people. People may choose to wear masks, even when they are not required. Respect the choices others make for their health.

Currently, proof of vaccination is no longer required in meetings in San Francisco. We will be monitoring that regulation and the ISSCC website will be updated as regulations change.

Hand sanitizing lotion will be available throughout the hotel and at the Registration desk.

REGISTRATION DESK HOURS:

Saturday, February 15:	**4:00 pm to 7:00 pm**
Sunday, February 16:	**7:00 am to 8:30 pm**
Monday, February 17:	**6:30 am to 4:00 pm**
Tuesday, February 18:	**8:00 am to 4:00 pm**
Wednesday, February 19:	**8:00 am to 4:00 pm**
Thursday, February 20:	**7:00 am to 2:00 pm**

Students must present their Student ID
at the Registration Desk to receive the student rates.

Those registering at the IEEE Member rate
must login to their IEEE membership during registration.

CONFERENCE INFORMATION

Deadlines: The deadline for registering at the Early Registration rates is 12:00 Midnight EST **Sunday January 12, 2025.** After January 12th, and before 12:00 Midnight EST **Monday January 27th, 2025,** registrations will be processed **at the Late Registration rates. After January 27th, you must register at the on-site rates.** You are urged to register early to obtain the lowest rates and ensure your participation in all aspects of ISSCC.

Cancellations/Adjustments: Prior to 12:00 Midnight EST **Monday January 27, 2025,** conference registration can be cancelled. Fees paid will be refunded (less a processing fee of $75). Send an email to the registration contractor at ISSCCinfo@yesevents.com to cancel or make other adjustments.

No refunds will be made after 12:00 Midnight EST January 27th, 2025. Paid registrants who do not attend the conference will have access to the on-demand material.

IEEE MEMBERSHIP SAVES ON ISSCC REGISTRATION

Take advantage of significantly reduced ISSCC fees by using your IEEE membership number. Additional savings are available for members of the IEEE Solid-State Circuits Society. If you're an IEEE member and have forgotten your member number, simply phone IEEE at 1(800) 678-4333 (US and Canada) or +1 732-981-0060 (all other regions) and ask. IEEE membership staff will take about two minutes to look up your number for you. If you come to register on site without your membership card, you can phone IEEE then, too. Or you can request a membership number look-up online at https://supportcenter.ieee.org. If you're not an IEEE member, consider joining before you register to save on your fees. Join online at www.ieee.org/join any time and you'll receive your member number by email. When joining IEEE you can also select a Solid-State Circuits Society (SSCS) membership, which more than pays for itself by giving you an additional $30 off the registration fee among other benefits.

SSCS MEMBERSHIP
A VALUABLE PROFESSIONAL RESOURCE FOR YOUR CAREER GROWTH

Stay Current! Get Connected! Invest in your Career! Membership in the Solid-State Circuits Society offers you the chance to explore solutions within a global community of colleagues in our field. Membership extends to you the opportunity to grow and share your knowledge, hone your expertise, expand or specialize your network of colleagues, advance your career, and give back to the profession and your local community.

SSCS MEMBERSHIP DELIVERS:

- Tools for Career growth
- Networking with peers
- Leadership opportunities
- Educational development
- Recognition for your achievements

We invite you to join or renew today to participate in exclusive educational events, access to leading research and best practice literature, and start your own career legacy by mentoring students and young professionals entering our field. It all starts with becoming a member of the Solid-State Circuits Society where you can:

-Keep up with the latest trends and cutting-edge developments in our industry - through our electronic newsletters, member magazine "Solid-State Circuits Magazine", and our award winning "Journal of Solid State Circuits".

-Access valuable career and educational tools - saving you both time and money with 24/7 access to our website and members-only professional development and educational material; Distinguished Lecturer Tours, Tutorials, and webinars by subject matter experts.

-Connect with your Peers - valuable networking opportunities through our world-class conferences, publication offerings, social media extensions, and interactive educational opportunities.

-Access exclusive SSCS Conference Digests for ISSCC, CICC, A-SSCC, ESSCIRC, and Symposium on VLSI Circuits.

-Access publications and EBooks - discounted access to vast online document libraries of journals, standards, and conference papers offer you one-third of the world's technical research to keep your knowledge current. Publications included in your SSCS membership are the "RFIC Virtual Journal" (RFVJ) and the "Journal on Exploratory Solid-State Computational Devices and Circuits" (JxCDC), Solid State Letters, and our newest Journal, the "Open Journal of the Solid-state Circuits Society" (OJ-SSCS) a fully open-access publication.

SSCS MEMBERSHIP SAVES EVEN MORE ON ISSCC REGISTRATION

This year, SSCS members will again receive an exclusive benefit of a $30 discount on the registration fee for ISSCC in addition to the IEEE discount. Also, the SSCS will again reward our members with a $10 Starbucks gift card when they attend the Conference as an SSCS member in good standing.

Join or renew your membership with IEEE's Solid-State Circuits Society today at sscs.ieee.org - you will not want to miss out on the opportunities and benefits your membership will provide now and throughout your career.

ITEMS INCLUDED IN REGISTRATION

Technical Sessions & more: In person registration includes admission to all technical and evening sessions starting Sunday evening and continuing throughout Monday, Tuesday and Wednesday. Access to author interviews, social hours, to the Student Research Preview, to the Demo Sessions, to the open Women in Circuits Programs and to the ~~new~~ Exhibition are also included. ISSCC does not offer partial conference registrations.

Technical Book Display: Several technical publishers will have collections of professional books and textbooks for sale during the Conference. The Book Display will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; on Tuesday from 3:00 pm to 8:00 pm; and on Wednesday from 10:00 am to 3:00 pm.

Exhibition: For the second year, ISSCC is planning to organize an Exhibition open to Companies and non-academic Research Institutions. The main aim of the Exhibition is to showcase the participating Corporations/Institutions, their products and their applications. The Exhibition will be open on Monday from 3:00 pm to 8:00 pm; on Tuesday from 9:30 am to 1:30 pm; and on Tuesday from 3:00 pm to 8:00 pm.

Demonstration Sessions: Hardware demonstrations will support selected papers on Monday and Tuesday evenings.

Author Interviews: Author Interviews will be held Monday, Tuesday and Wednesday evenings. Authors from each day's papers will be available to discuss their work.

Monday and Tuesday Social Hours: Refreshments will be available starting at 5:30 pm.

University Events: Several universities are planning social events during the Conference. Check the University Events display at the conference for the list of universities, locations and times of these events.

Publications: All ISSCC registrants will be able to access online the Digital Digest and the registrations of the Technical Presentations Besides, Conference registration includes:

-Papers Visuals: The visuals from all papers presented will be available by download.

-Demonstration Session Guidebook: A descriptive guide to the Demonstration Session will be available by download.

-Note: Instructions will be provided for access to all downloads. Downloads will be available both during the Conference and for a limited time afterwards.

OPTIONAL EVENTS

Educational Events: Many educational events are available at ISSCC for an additional fee. There are ten 90-minute Tutorials and two all-day Forums on Sunday. There are four additional all-day Forums on Thursday as well as an all-day Short Course. The Forums and Short Course include breakfast pastries and coffee, lunch and break refreshments. The Tutorials include break refreshments. See the schedule for details of the topics and times.

OPTIONAL PUBLICATIONS

ISSCC 2025 Publications: The following ISSCC 2025 digital publications can be purchased in advance or on site:

2025 ISSCC Download USB: All of the downloads included in conference registration, (regular papers and presentations) **(mailed in March)**

2025 Tutorials USB: All of the 90 minute Tutorials **(mailed in June).**

2025 Short Course USB: (mailed in June).
The Short Course and Tutorial USBs contain audio and written English transcripts synchronized with the presentation visuals. In addition, the USBs contain a pdf file of the presentations and pdf files of key reference material.

Earlier ISSCC Publications: Selected publications from earlier conferences can be purchased. There are several ways to purchase this material:

-Items listed on the registration website can be purchased with registration and picked up at the conference.

-Visit the ISSCC Publications Desk. This desk is located in the registration area and has the same hours as conference registration. With payment by cash, check or credit card, you can purchase materials at this desk. See the posted list at the Conference for titles and prices.

-Visit the ISSCC website at www.isscc.org and click on the link "SHOP/Shop ISSCC/Shop Now" where you can order online or download an order form to mail, email or fax. For a small shipping fee, this material will be sent to you immediately and you will not have to wait until you attend the Conference to get it.

HOW TO MAKE HOTEL RESERVATIONS

Online: ISSCC participants are urged to make their hotel reservations at the San Francisco Marriott Marquis online. Go to the conference website and click on the Hotel Reservation link. ***Conference room rates are $285 for a single/double*** *(per night plus tax).* In addition, ISSCC attendees who are Bonvoy Members booked in the ISSCC group receive **in-room Internet access. Non-members of Bonvoy may sign up at check in, there is no charge for participation.**

All online reservations require the use of a credit card. Online reservations are confirmed immediately. You should print the page containing your confirmation number and reservation details and bring it with you when you travel to ISSCC. **Telephone:** Call 877- 622-3056 (US) or 415-896-1600 and ask for "Reservations." When making your reservation, identify the group as ISSCC 2025 to get the group rate.

Hotel Deadline: Reservations must be received at the San Francisco Marriott Marquis no later than 5 pm Pacific Time January 27th, 2025 to obtain the special ISSCC rates. A limited number of rooms are available at these rates. **Once this limit is reached or after January 27th, the group rates may no longer be available and reservations will be filled at the best available rate.** Changes: Before the hotel deadline, your reservation can be changed by calling the telephone numbers above. After the hotel deadline, call the Marriott Marquis at 415-896-1600 (ask for "Reservations"). Have your hotel confirmation number ready.

IEEE NON-DISCRIMINATION POLICY

IEEE is committed to the principle that all persons shall have equal access to programs, facilities, services, and employment without regard to personal characteristics not related to ability, performance, or qualifications as determined by IEEE policy and/or applicable laws.

EVENT PHOTOGRAPHY

Attendance at, or participation in, this conference constitutes consent to the use and distribution by IEEE of the attendee's image or voice for informational, publicity, promotional and/or reporting purposes in print or electronic communications media. Video or audio recording by participants or other attendees during any portion of the conference is not allowed without special prior written permission of IEEE.

TAKING PICTURES, VIDEOS OR AUDIO RECORDINGS DURING ANY OF THE SESSIONS IS NOT PERMITTED

REFERENCE INFORMATION

Conference Website:	www.isscc.org
ISSCC Email:	ISSCC@ieee.org
Registration questions:	ISSCCinfo@yesevents.com
Hotel Information:	San Francisco Marriott Marquis Phone: 415-896-1600 780 Mission Street San Francisco, CA 94103
Press Information:	Laura C. Fujino Phone: 416-418-3034 University of Toronto Email: lcfujino@aol.com
Registration:	YesEvents Phone: 800-937-8728 Email: issccinfo@yesevents.com

Hotel Transportation

Visit the ISSCC website "Registration/Transportation from Airport" page for helpful travel information and links.
You can get a map and driving directions from the hotel website at:
www.marriott.com/hotels/travel/sfodt-san-francisco-marriott-marquis/

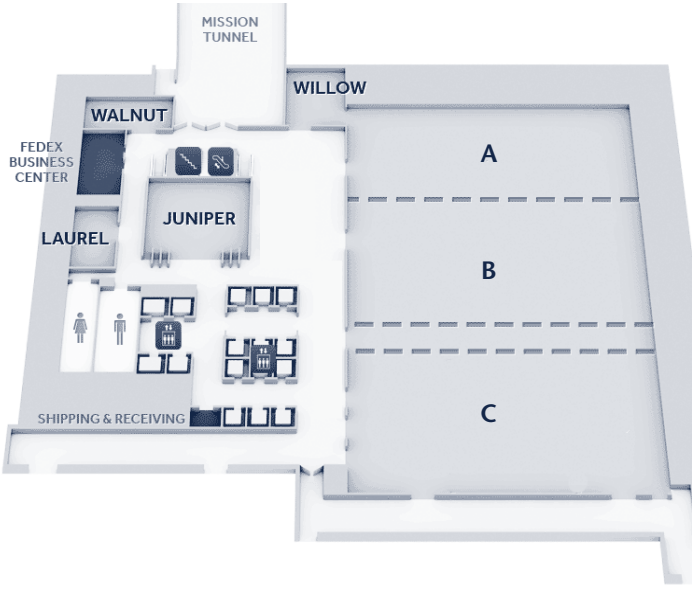
Next ISSCC Dates and Location:
ISSCC 2026 will be held on February 15-19, 2026
at the San Francisco Marriott Marquis Hotel.

Subcommittee Chairs

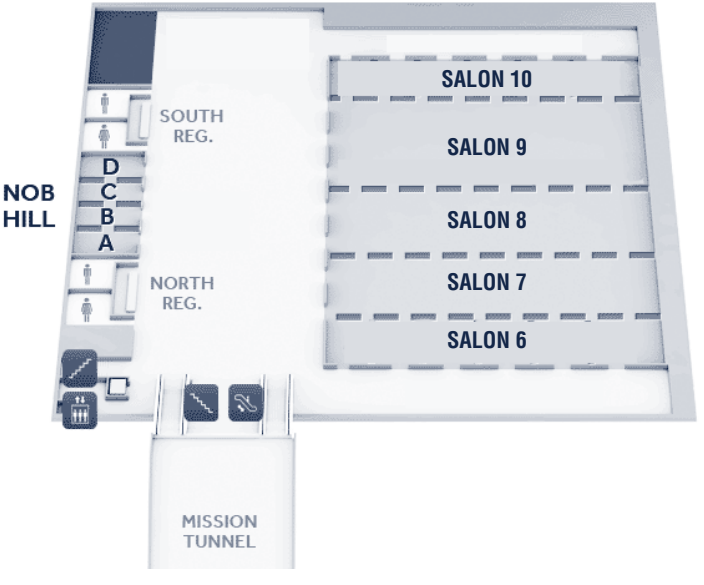
Analog:	Viola Schaffer
Data Converters:	Jan Westra
Digital Architectures & Systems:	Rahul Rao
Digital Circuits:	Huichu Liu
Imagers, MEMS, Medical & Displays:	Rikky Muller
Memory:	Meng-Fan Chang
Power Management:	Bernhard Wicht
Power Management:	Saurev Bandyopathy-Vice-Chair
RF:	Brian Ginsburg
RF:	Massoud Babie-Vice-Chair
Security:	Ingrid Verbauwhede
Technology Directions:	Ali Hajimiri
Wireless:	Chih-Ming Hung
Wireline:	Thomas Toifl

Program-Committee Chair:	Thomas Burd
Program-Committee Vice-Chair:	Keith Bowman
Conference Chair:	Edith Beigné

B2 Level
Golden Gate Hall



Lower B2 Level
Yerba Buena Ballroom



445 Hoes Lane
P.O. Box 1331
Piscataway, NJ 08855-1331
USA

ISSCC.org

sscs.ieee.org

ISSCC 2025 ADVANCE PROGRAM